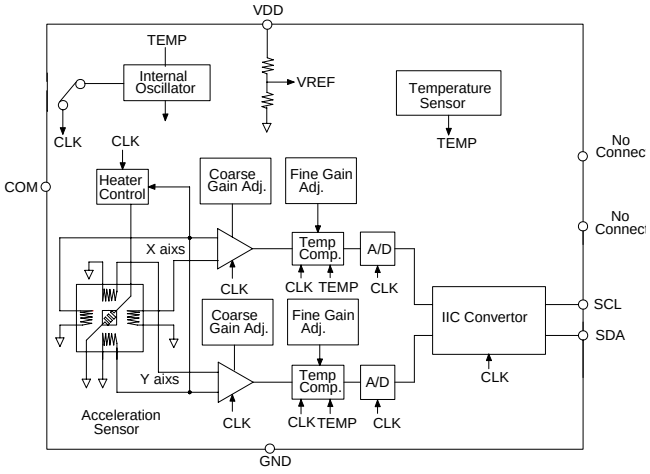
Ultra High Performance ±1.5 *g* Dual Axis Accelerometer with I²C Interface

MXC6225xQ

FEATURES

RoHS compliant
I²C Slave, FAST (≤400 KHz) mode interface
1.8V compatible I/O
Ultra Low Noise and initial offset
Embedded Power up/down function
On-chip temperature sensor available
Eight, customer defined 7-bit addresses
2.7 V to 3.6 V single supply continuous operation
Monolithic CMOS IC
Low power consumption: typically <2 mA @ 3.0 V
Resolution better than 1 mg
On chip mixed signal processing
>50,000 *g* shock survival rating
Low profile LCC package: 5mm X 5mm X 1.55mm



MXC6225xQ FUNCTIONAL BLOCK DIAGRAM

APPLICATIONS

Security – Gas Line/Elevator/Fatigue Sensing

Gaming – Joystick/RF Interface/Menu Selection/Tilt Sensing

GPS – Electronic Compass Tilt Correction, Dead Reckoning

Consumer – LCD Projectors, Pedometers, Blood Pressure Monitor, Digital Cameras

Information Appliances – Computer Peripherals/PDA's/Mouse Smart Pens/Cell Phones

GENERAL DESCRIPTION

The MXC6225xQ is a low cost, dual axis accelerometer fabricated on a standard, submicron CMOS process. It is a complete sensing system with on-chip mixed signal processing. The MXC6225xQ measures acceleration with a full-scale range of ±1.5 *g* and a sensitivity of 512counts/g at @3.0 V at 25°C. It can measure both dynamic acceleration (e.g. vibration) and static acceleration (e.g. gravity). The MXC6225xQ design is based on heat convection and requires no solid proof mass.

This design eliminates the stiction problems associated with legacy technologies and provides shock survival greater than 50,000*g's*.

Memsic's solid state design leads to significantly lower failure rates in customer applications and lower loss due to handling during manufacturing and assembly processes

The MXC6225xQ provides I²C digital output with 400 KHz. fast mode operation.

The typical noise floor is 0.13 mg/$\sqrt{Hz}$ allowing signals below 0.5m*g* to be resolved at 1 Hz bandwidth.

The MXC6225xQ is packaged in a hermetically sealed, low profile LCC surface mount package (5 mm x 5 mm x 1.55 mm) and is available in operating temperature ranges of -40°C to +105°C.

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ELECTRICAL CHARACTERISTICS (Measurements @ 25°C, Acceleration = 0 *g* unless otherwise noted; V_{DD} = 3.0V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Measurement Range[1]	Each Axis	±1.5			*G*
Nonlinearity	Best fit straight line		0.5	1.0	% of FS
Alignment Error[2]			±1.0		degrees
Transverse Sensitivity[3]			±2.0		%
Sensitivity		486	512	538	counts/g
Sensitivity Change Over Temperature	Δ from 25°C at -40°C Δ from 25°C at 105°C	 -60		160	%
Zero *g* Offset Bias Level		-0.05 2022	0.0 2048	+0.05 2074	*g* counts
Zero *g* Offset TC	Δ from 25°C		0.1	0.5	m*g*/°C
Tout		3195	3375	3555	counts
Tout Sensitivity		0.18	0.22	0.26	°C/count
Noise Density, RMS			0.15		$mg/\sqrt{Hz}$
Resolution	@ 1Hz. BW		0.2	0.5	mg
Frequency Response	@ -3dB	6	8	10	Hz
Output Drive Capability	@ 2.7 V – 3.6 V			100	µA
Turn-On Time[4]			150	200	mS
Operating Voltage Range		2.7	3.0	3.6	V
Supply Current			1.8		mA
Power Down Current				1.0	µA
Operating Temperature Range		-40		+105	°C

NOTES:

[1] Guaranteed by measurement of initial offset and sensitivity

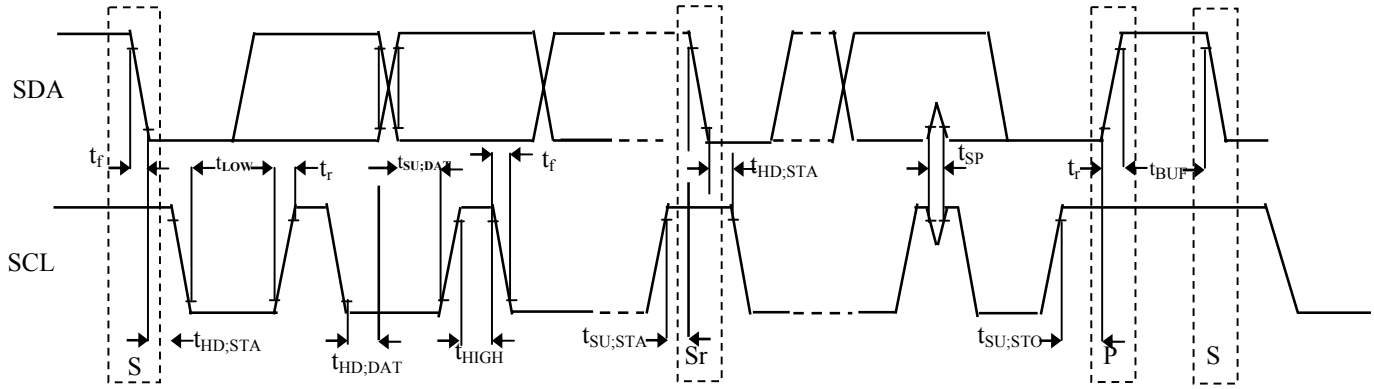
[2] Alignment error is specified as the angle between the true and indicated axis of sensitivity

[3] Cross axis sensitivity is the algebraic sum of the alignment and the inherent sensitivity errors

[4] Output settled to within ± 17mg

I²C INTERFACE I/O CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	V_{IL}		-0.5		$0.3*V_{DD2}$	V
Logic Input High Level	V_{IH}		$0.7*V_{DD2}$		V_{DD2}	V
Hysteresis of Schmitt input	V_{hys}		0.2			V
Logic Output Low Level	V_{OL}				0.4	
Input Leakage Current	I_i	$0.1V_{DD2}<V_{in}<0.9$ V_{DD2}	-10		10	µA
SCL Clock Frequency	f_{SCL}		0		400	kHz
START Hold Time	$t_{HD;STA}$		0.6			µS
START Setup Time	$t_{SU;STA}$		0.6			µS
LOW period of SCL	t_{LOW}		1.3			µS
HIGH period of SCL	t_{HIGH}		0.6			µS
Data Hold Time	$t_{HD;DAT}$		0		$0.7* t_{LOW}$	µS
Data Setup Time	$t_{SU;DAT}$		0.1			µS
Rise Time	t_r	From V_{IL} to V_{IH}			0.3	µS
Fall Time	t_f	From V_{IH} to V_{IL}			0.3	µS
Bus Free Time Between STOP and START	t_{BUF}		1.3			µS
STOP Setup Time	$t_{SU;STO}$		0.6			µS



Timing Definition

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) ……...-0.5 V to +7.0V

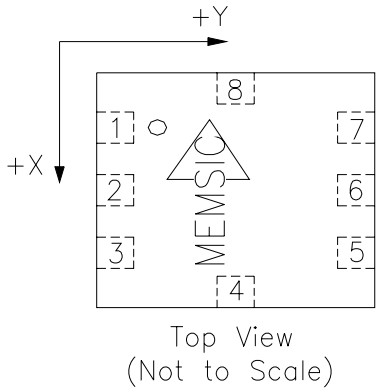
Storage Temperature ……..……-65°C to +150°C

Acceleration ……..50,000 *g*

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description: LCC-8 Package

Pin	Name	Description	I/O
1	NC	Do Not Connect	NC
2	COM	Connected to Ground	I
3	GND	Connected to Ground	I
4	TEST	Do Not Connect	NC
5	VDD2	Power Supply for I^2C bus	I
6	SCL	Serial Clock Line for I^2C bus	I
7	SDA	Serial Data Line for I^2C bus	I/O
8	V_{DD}	2.7 V to 3.6 V	I



Note: The MEMSIC logo's arrow indicates the -X sensing direction of the device. The +Y sensing direction is rotated 90° away from the +X direction following the right-hand rule. Small circle indicates pin one (1).

Ordering Guide

MXC6225xQB

Package type:

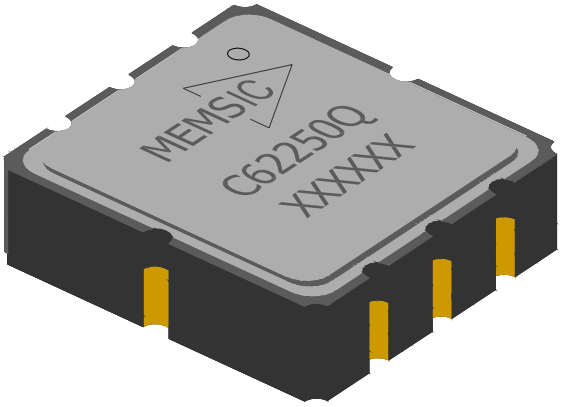
Code	Type
B	LCC8, Pb-free RoHS compliant

Performance Grade:

Code	Temp	Resolution
Q	-40~105°C	4096counts

Address code: 0~7

Number	Address
0	20H
1	22H
2	24H
3	26H
4	28H
5	2AH
6	2CH
7	2EH



All parts are shipped in tape and reel packaging.

Caution: ESD (electrostatic discharge) sensitive device.

THEORY OF OPERATION

The MEMSIC device is a complete dual-axis acceleration measurement system fabricated on a monolithic CMOS IC process. The device operation is based on heat transfer by natural convection and operates like other accelerometers except it is a gas in the MEMSIC sensor.

A single heat source, centered in the silicon chip is suspended across a cavity. Equally spaced aluminum/polysilicon thermopiles (groups of thermocouples) are located equidistantly on all four sides of the heat source (dual axis). Under zero acceleration, a temperature gradient is symmetrical about the heat source, so that the temperature is the same at all four thermopiles, causing them to output the same voltage.

Acceleration in any direction will disturb the temperature profile, due to free convection heat transfer, causing it to be asymmetrical. The temperature, and hence voltage output of the four thermopiles will then be different. The differential voltage at the thermopile outputs is directly proportional to the acceleration. There are two identical acceleration signal paths on the accelerometer, one to measure acceleration in the x-axis and one to measure acceleration in the y-axis. Please visit the MEMSIC website at www.memsic.com for a picture/graphic description of the free convection heat transfer principle.

MXC6225Q PIN DESCRIPTIONS

VDD – This is the supply input for the circuits and the sensor heater in the accelerometer. The DC voltage should be between 2.7 and 3.6 volts. Refer to the section on PCB layout and fabrication suggestions for guidance on external parts and connections recommended.

GND– This is the ground pin for the accelerometer.

COM– This pin should be connected to ground.

TEST– Do Not Connect, factory use only.

VDD2– This pin is the I^2C input digital power supply, the voltage on this pin determines the I^2C bus logic voltage, and is 1.8V compatible. Note: The voltage on this pin should never go higher than the voltage on V_{DD}, if VDD2 has a lower power supply voltage than V_{DD}, power should be applied to V_{DD} first.

SDA– This pin is the I^2C serial data line, and operates in FAST (400 KHz.) mode.

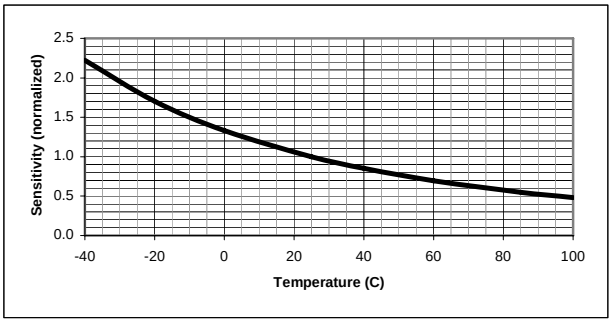
SCL– This pin is the I^2C serial clock line, and operates in FAST (400 KHz.) mode.

COMPENSATION FOR THE CHANGE IN SENSITIVITY OVER TEMPERATURE

All thermal accelerometers display the same sensitivity change with temperature. The sensitivity change depends on variations in heat transfer that are governed by the laws of physics. The sensitivity change is governed by the following equation (and shown in following figure in °C):

$$S_i \times T_i^{3.3} = S_f \times T_f^{3.3}$$

where S_i is the sensitivity at any initial temperature T_i, and S_f is the sensitivity at any other final temperature T_f with the temperature values in °K.



Thermal Accelerometer Sensitivity

In gaming applications where the game or controller is typically used in a constant temperature environment, sensitivity might not need to be compensated in hardware or software. Any compensation for this effect could be done instinctively by the game player.

For applications where sensitivity changes of a few percent are acceptable, the above equation can be approximated with a linear function. Using a linear approximation, an external circuit that provides a gain adjustment of –1.1%/°C would keep the sensitivity within 10% of its room temperature value over a 0°C to +50°C range.

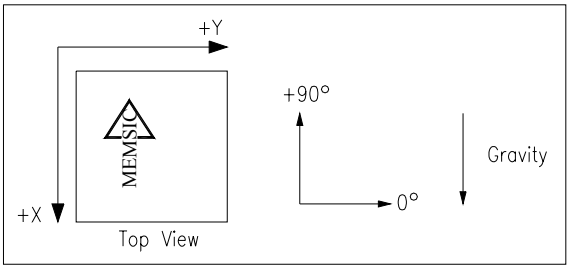
For applications that demand high performance, a low cost micro-controller can be used to implement the above equation. A reference design using a Microchip MCU (p/n 16F873/04-SO) and MEMSIC developed firmware is available by contacting the factory. With this reference design, the sensitivity variation over the full temperature range (-40°C to +105°C) can be kept below 3%. Please visit the MEMSIC web site at www.memsic.com for reference design information on circuits and programs including look up tables for easily incorporating sensitivity compensation.

DISCUSSION OF TILT APPLICATIONS AND RESOLUTION

Tilt Applications: One of the most popular applications of the MEMSIC accelerometer product line is in tilt/inclination measurement. An accelerometer uses the force of gravity as an input to determine the inclination angle of an object.

A MEMSIC accelerometer is most sensitive to changes in position, or tilt, when the accelerometer's sensitive axis is perpendicular to the force of gravity, or parallel to the Earth's surface. Similarly, when the accelerometer's axis is parallel to the force of gravity (perpendicular to the Earth's surface), it is least sensitive to changes in tilt.

Following table and figure help illustrate the output changes in the X- and Y-axes as the unit is tilted from +90° to 0°. Notice that when one axis has a small change in output per degree of tilt (in m*g*), the second axis has a large change in output per degree of tilt. The complementary nature of these two signals permits low cost accurate tilt sensing to be achieved with the MEMSIC device (reference application note AN-00MX-007).



Accelerometer Position Relative to Gravity

X-Axis Orientation To Earth's Surface (deg.)	X-Axis		Y-Axis	
	X Output (*g*)	Change per deg. of tilt (m*g*)	Y Output (*g*)	Change per deg. of tilt (m*g*)
90	1.000	0.15	0.000	17.45
85	0.996	1.37	0.087	17.37
80	0.985	2.88	0.174	17.16
70	0.940	5.86	0.342	16.35
60	0.866	8.59	0.500	15.04
45	0.707	12.23	0.707	12.23
30	0.500	15.04	0.866	8.59
20	0.342	16.35	0.940	5.86
10	0.174	17.16	0.985	2.88
5	0.087	17.37	0.996	1.37
0	0.000	17.45	1.000	0.15

Changes in Tilt for X- and Y-Axes

RESOLUTION

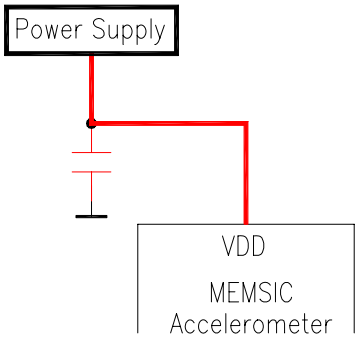
The accelerometer resolution is limited by noise. The output noise will vary with the measurement bandwidth. With the reduction of the bandwidth, by applying an external low pass filter, the output noise drops. Reduction of bandwidth will improve the signal to noise ratio and the resolution. The output noise scales directly with the square root of the measurement bandwidth. The maximum amplitude of the noise, its peak- to- peak value, approximately defines the worst case resolution of the measurement. With a simple RC low pass filter, the rms noise is calculated as follows:

$$\text{Noise (mg rms)} = \text{Noise(mg/}\sqrt{Hz}\text{)} * \sqrt{(Bandwidth(Hz) * 1.6)}$$

The peak-to-peak noise is approximately equal to 6.6 times the rms value (for an average uncertainty of 0.1%).

HARDWARE DESIGN CONSIDERATION

1. One capacitor is recommended for best rejection of power supply noise (reference figure below). The capacitor should be located as close as possible to the device supply pin (V_{DD}). The capacitor lead length should be as short as possible, and a surface mount capacitor is preferred. For typical applications, the capacitor can be ceramic 0.1 µF.



Power supply noise rejection

2. Robust low inductance ground wiring should be used.
3. Care should be taken to ensure there is "thermal symmetry" on the PCB immediately surrounding the MEMSIC device and that there is no significant heat source nearby. Based on the experiment, with a 120degC heating source at 11mm away of MEMSIC device, the offset change will be within 5mg.
4. A metal ground plane should be added directly beneath the MEMSIC device. The size of the plane should be similar to the MEMSIC device's footprint and be as thick as possible.
5. Vias can be added symmetrically around the ground plane. These vias will increase the thermal isolation of the device from the rest of the PCB and improve performance.

SOFTWARE DESIGN CONSIDERATION

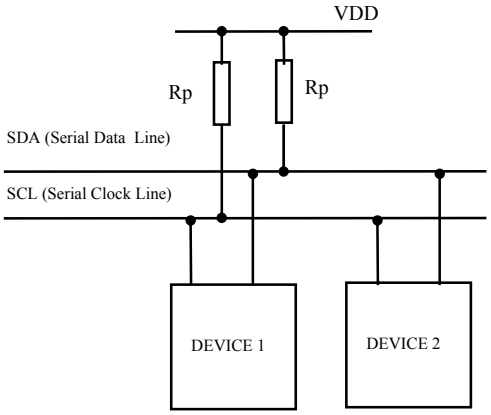
A register or flag is required between I^2C MCU (the master device) and any system level CPU/MCU (if there exists any system level controller (such as a PC based system). The potential issue will be that system level controller may read in MSB and LSB of the same axis from different events of on-chip A/D conversions, since I^2C data length is 8 bits while the sensor has data length of 12 bits.

I^2C INTERFACE DESCRIPTION

A slave mode I^2C circuit has been implemented into the Memsic thermal accelerometer as a standard interface for customer applications. The A/D converter and MCU functionality have been added to the Memsic sensor, thereby increasing ease-of-use, and lowering power consumption, footprint and total solution cost.

The I^2C (or Inter IC bus) is an industry standard bi-directional two-wire interface bus. A master I^2C device can operate READ/WRITE controls to an unlimited number of devices on the bus by proper addressing. The Memsic accelerometer operates only in a slave mode, i.e. only responding to calls by a master device

I^2C BUS CHARACTERISTICS



I^2C bus

The two wires in I^2C bus are called SDA (serial data line) and SCL (serial clock line). In order for a data transfer to start, the bus has to be free, which is defined by both wires in a HIGH output state. Due to the open-drain/pull-up resistor structure and wire-AND operation, any device on the bus can pull lines low and overwrite a HIGH signal. The data on the SDA line has to be stable during the HIGH period of the SCL line. In other words, valid data can only change when the SCL line is LOW.

Note: Rp selection guide: 4.7Kohm for a short I^2C bus length (less than 4inches), and 10Kohm for less than 2inches I^2C bus.

I^2C BUS DATA TRANSFER

A data transfer is started with a "START" condition and ended with a "STOP" condition. A "START" condition is defined by a HIGH to LOW transition on the SDA line while SCL line is HIGH. A "STOP" condition is defined by a LOW to HIGH transition on the SDA line while SCL line is HIGH. All data transfer in I^2C system is 8-bits long. Each byte has to be followed by an acknowledge bit. Each data transfer involves a total of 9 clock cycles. Data is transferred starting with the most significant bit (MSB). After a "START" condition, master device calls a specific slave device, in our case, the Memsic accelerometer with a 7-bit device address. To avoid potential address conflict, either by ICs from other manufacturers or by other Memsic accelerometers on the same bus, a total of 8 different addresses can be programmed into a Memsic device at the factory.

Following the 7-bit address, the 8^{th} bit determines the direction of data transfer: [1] for READ and [0] for WRITE. After being addressed, the available Memsic device being called will respond by an "Acknowledge" signal, which is pulling SDA line LOW.

In order to read an acceleration signal, the master device should operate a WRITE action with a code of [xxxxxxx0] into the Memsic device 8-bit internal register.

Bit	Name	Function
0	PD (Power Down)	Power down [1]/on [0]
1	Reserved	Set to "0"
2	BGTST (bandgap test)	Bandgap test [1]/normal[0]
3	TOEN (temperature out enable)	Temp Out EN [1]/disable[0]
4	Reserved	Fixed to 0
5	Reserved	
6	Reserved	
7	Reserved	

BGTST is used to calibrate the temperature output signal's initial offset. By flipping the BGTST bit and taking the average of two readings, the temperature output initial offset will be calibrated to within datasheet specifications.

After writing code of [xxxxxxx0] into the control register, if a "READ" signal is received, during next 9 clock cycles, the Memsic device being called will transfer 8-bits of data to the I^2C bus. If an "Acknowledge" by master device is received, the Memsic device will continue to transfer the next byte. The same procedure repeats until 5 bytes of data are transferred to master device. Those 5 bytes of data are defined as following ("T" is temperature output):

1. Internal register
2. MSB X/T axis
3. LSB X/T axis
4. MSB Y axis
5. LSB Y axis

Even though each axis consists of two bytes, which are 16-bits of data, the actual accelerometer resolution is limited to 12 bits. Unused MSB's will be simply filled by "0"s.

Note that temperature output shares the same registers with X channel output. Customer can select which signal needs to be read out by using TOEN bit.

Note: 20mS typical waiting time is necessary between each data acquisition.

The master can stop slave data transfer after any of the five bytes by not sending an acknowledge command and followed by a "STOP" condition.

POWER DOWN MODE

The Memsic accelerometer can enter a power down mode by the master device writing a code of [xxxxxxx1] into the accelerometer's internal register. A wake up operation is performed when the master writes into the same register a code of [xxxxxxx0]. Note that the MXC6225xQ needs about 150mS (typical) for power up time.

EXAMPLE OF DATA COMMUNICATION

First cycle: START followed by a calling to slave address [0010xxx] to WRITE (8^{th} SCL, SDA keep low). [xxx] Is determined by factory programming, a total of 8 different addresses are available.

Second cycle: After an acknowledge signal is received by the master device (Memsic device pulls SDA line low during 9^{th} SCL pulse), master device sends "[00000000]" as the target address to be written into. Memsic device should acknowledge at the end (9^{th} SCL pulse). Note: since Memsic device has only one internal register that can be written into, user should always indicate "[00000000]" as the write address.

Third cycle: Master device writes to internal Memsic device memory code "[xxx0xxx0]" as a wake-up call. The Memsic device should send acknowledge signal. A STOP command indicates the end of write operation. A 150mS (typical) wait period should be given to Memsic device to return from a power-down mode. The delay value depends on the type of Memsic device. Generally speaking, low power products tend to have longer startup time.

Fourth cycle: Master device sends a START command followed by calling Memsic device address with a WRITE (8^{th} SCL, SDA keep low). An "acknowledge" should be sent by Memsic device at the end.

Fifth cycle: Master device writes to Memsic device a "[00000000]" as the starting address for which internal memory is to be read. Since "[00000000]" is the address of internal control register, reading from this address can serve as a verification of operation and to confirm the write command has been successful. Note: the starting address in principle can be any of the 5 addresses. For example, user can start read from address [0000001], which is X channel MSB.

Sixth cycle: Master device calls Memsic device address with a READ (8^{th} SCL cycle SDA line high). Memsic device should acknowledge at the end.

Seventh cycle: Master device cycles SCL line, first addressed memory data appears on SDA line. If in step 7, "[00000000]" was sent, internal control register data should appear (in the following steps, this case is assumed). Master device should send acknowledge at the end.

Eighth cycle: Master device continues cycle SCL line, next byte of internal memory should appear on SDA line (MSB of X channel). The internal memory address pointer automatically moves to the next byte. Master acknowledges.

Ninth cycle: LSB of X channel. In the case that TOEN bit of internal register was set to "1", the MSB and LSB of TOUT (temperature) should appear in last two steps.

Tenth cycle: MSB of Y channel.

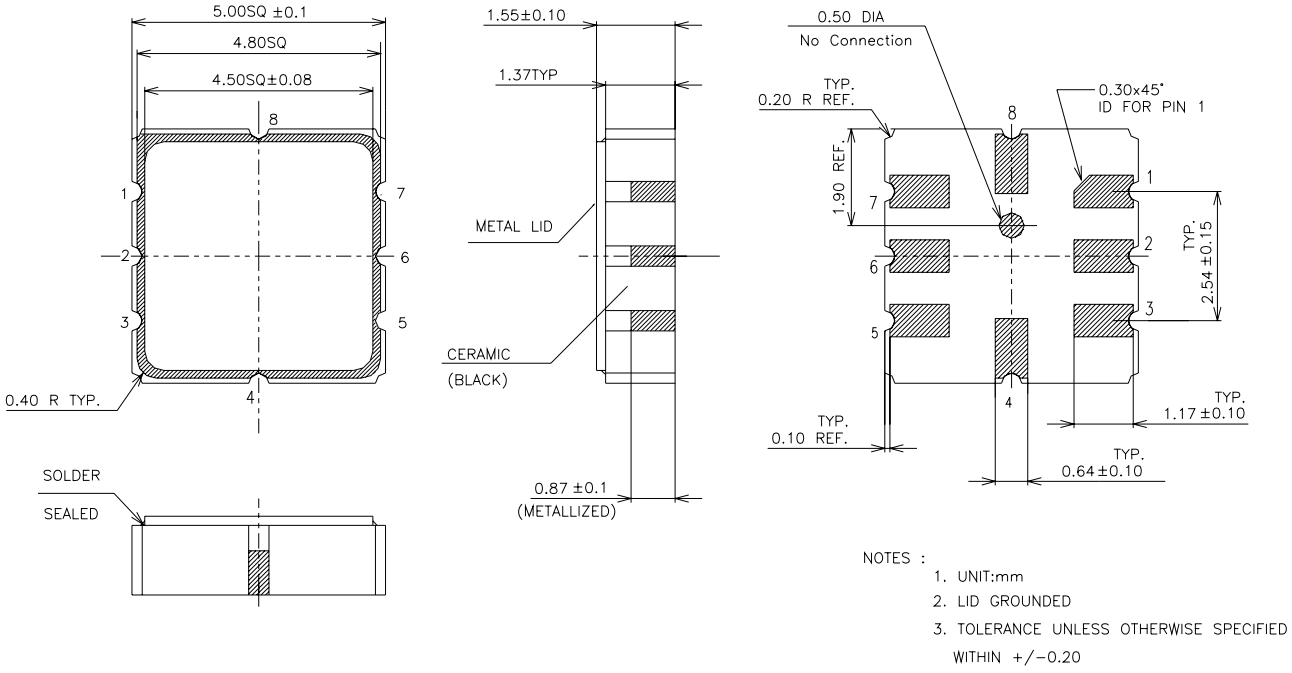
Eleventh cycle: LSB of Y channel.

Master ends communications by sending NO acknowledge and followed by a STOP command. Note: if mater device continues to cycle SCL line, the memory pointer will go to sixth and seventh positions, which always have "[00000000]". After seventh position, pointer will go to zero again.

Optional: Master power down Memsic device by writing into internal control register. (See step 1 through 4 for WRITE operation)

Note: at power-on, internal register and memory address pointer are reset to all "0".

LCC-8 PACKAGE DRAWING



Hermetically Sealed Package Outline