GENERAL DESCRIPTION

The MC6470 combines a 6 DoF (6 Degrees of Freedom) accelerometer and magnetometer sensor solution in 2x2mm single package for the consumer electronics market.

The MC6470 has a linear acceleration full-scale range of ±16g and a low noise magnetic sensor with up to 0.15μT magnetic field resolution. A single I2C interface is available to separately control magnetometer and accelerometer functions, enabling independent operation of functions for application flexibility.

TARGET APPLICATIONS

- Pedometers
- Tap/double-Tap recognition
- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection

FEATURES

- Competitive 6 DoF solution
  - 3-axis accelerometer sensor
  - 3-axis magnetometer sensor
- 2x2mm single package
  - 2 × 2 × 0.95mm 12-pin LGA
  - Industry leading 6 DoF package
- Flexible pin compatibility
  - MEMSIC 3-axis accelerometer MC34xx
- High performance eCompass
  - 3-axis magnetometer and 3-axis accelerometer
  - Single I2C interface to 400 kHz
- Magnetometer
  - High performance magnetic sensor with 0.15μT resolution
  - 0.35uT Noise
  - 15-bit resolution
  - Broad field range up to ±2.4mT
  - Programmable output data rate from 0.5 to 100 Hz
- Accelerometer
  - ±2,4,8,16g full-scale acceleration range
  - 14-bit resolution

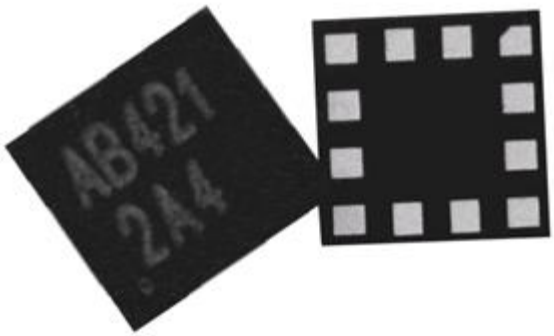

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TABLE OF CONTENTS

1 ORDER INFORMATION

Part Number	Resolution	Order Number	Package	Shipping
MC6470	14-bit	MC6470	LGA12	Tape & Reel, 5Ku

Table 1. Order Information

2 FUNCTIONAL BLOCK DIAGRAM

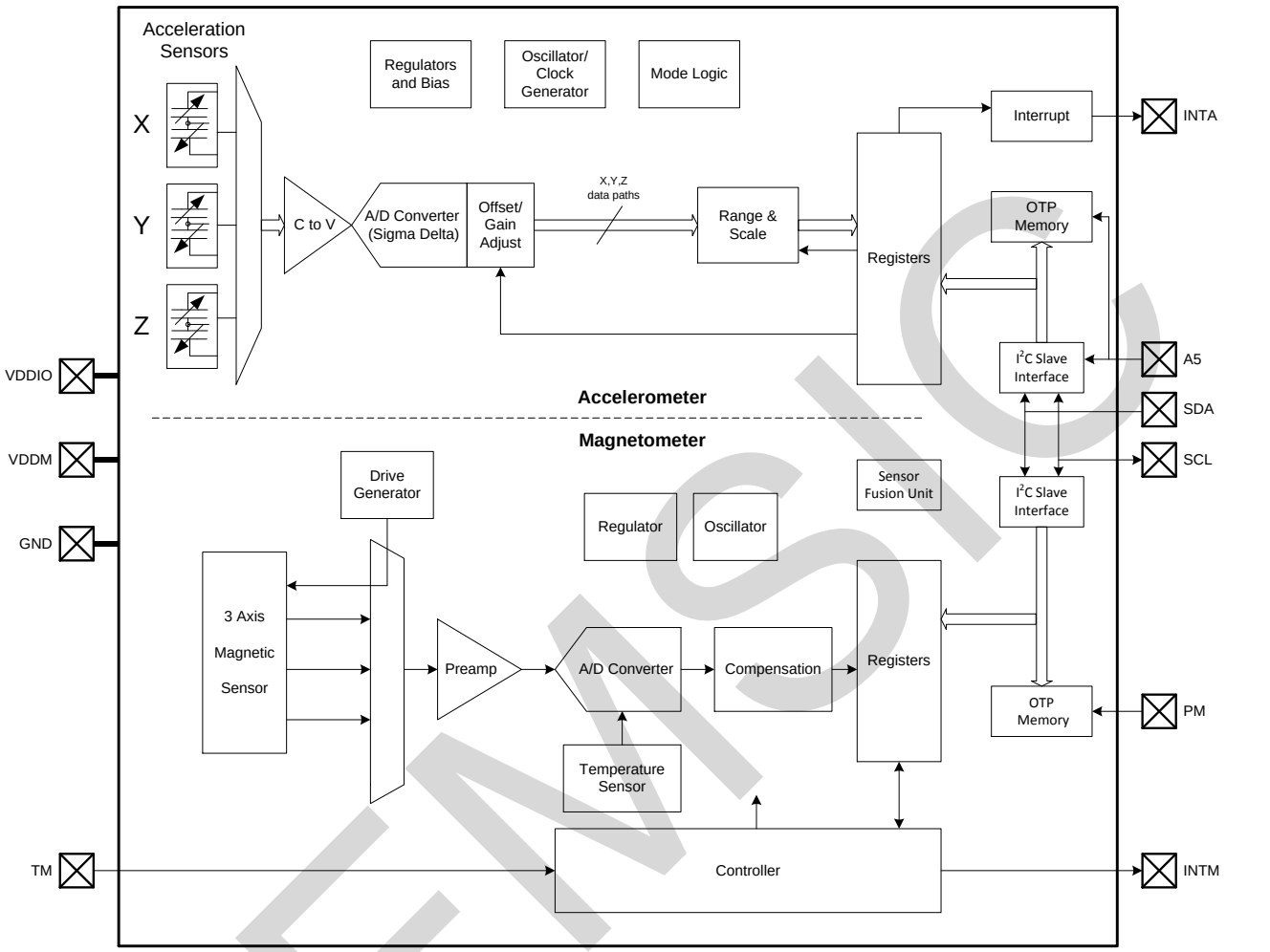


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTIONS

3.1 Package Orientation

Positive values indicate direction of acceleration force.

The magnetic sensor output value of each axis is positive when turned toward magnetic north.

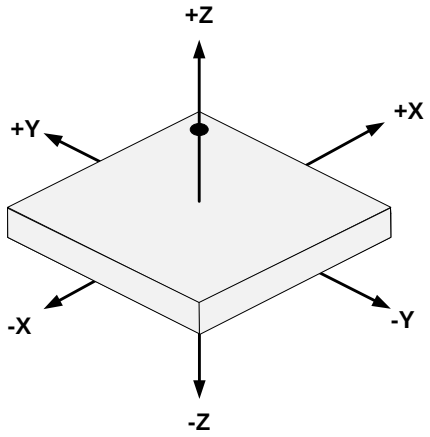


Figure 2. Package Axis Reference – Magnetometer & Accelerometer

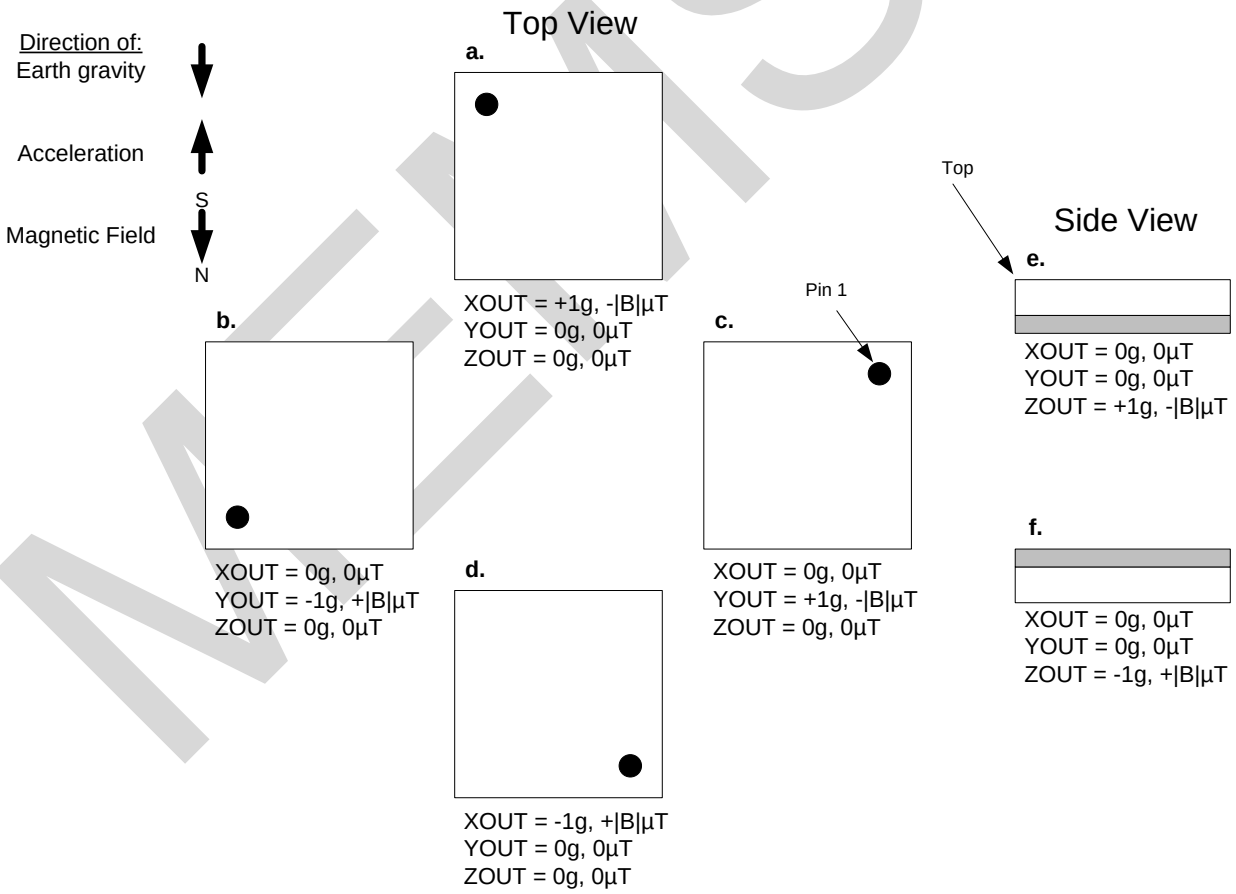


Figure 3. Package Orientation – Accelerometer & Magnetometer

3.2 Package Outline

Dimension in millimeters				Dimension in millimeters			
Ref	Min.	Nom.	Max.	Ref	Min.	Nom.	Max.
A	1.9	2	2.1	E1	0.47	0.50	0.53
B	1.9	2	2.1	E2	---	0.375	---
C	0.90	0.95	1.00	E3	---	0.1	---
C1	0.80	0.85	0.90				
C2	0.07	0.10	0.13				
D1	0.22	0.25	0.28				
D2	0.240	0.270	0.300				
D3	0.47	0.50	0.53				
D4	---	0.625	---				
D5	---	0.1	---				

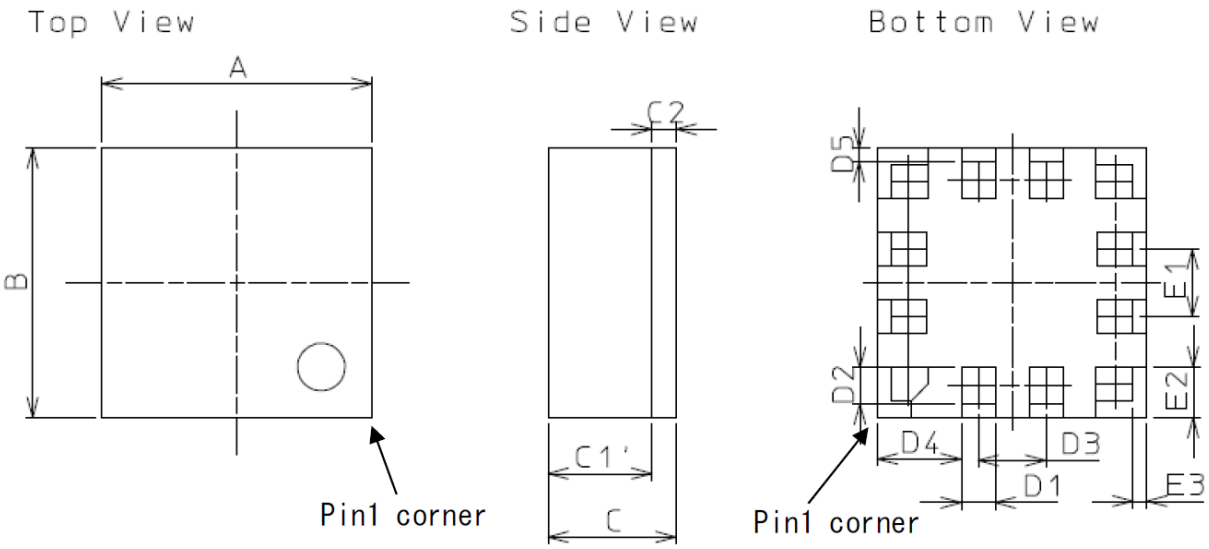


Figure 4. Package Outline Dimensions

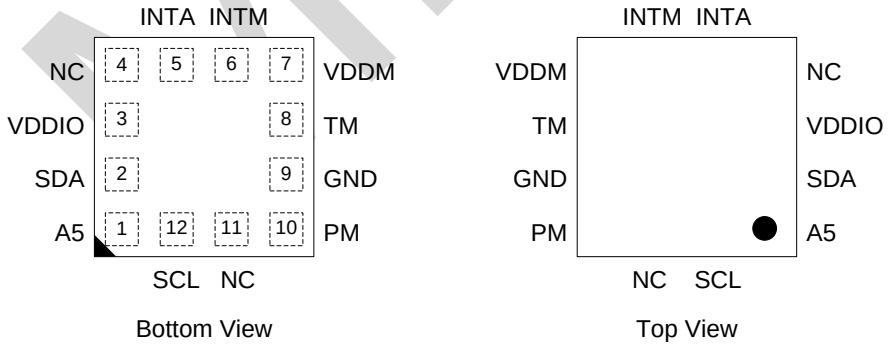


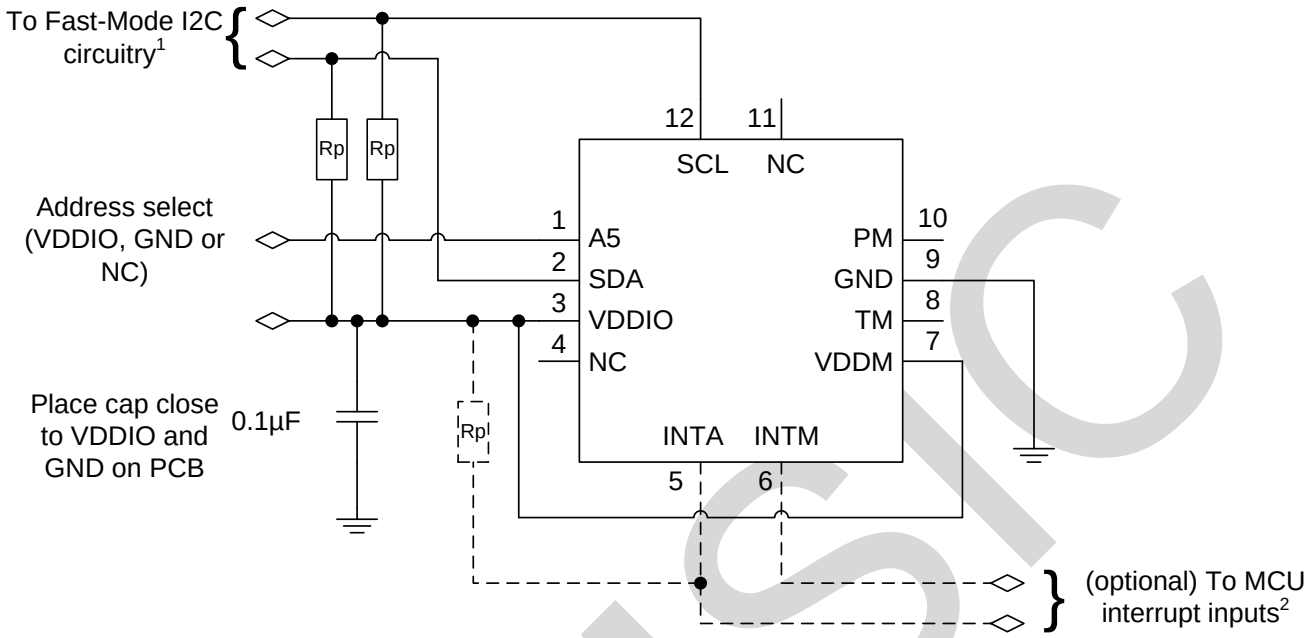
Figure 5. Package Pins

3.3 Pin Descriptions

Pin	Name	Function
1	A5	Accelerometer I2C Address Select and Factory Program (NC/GND/VDDIO)
2	SDA	I2C Serial Data Input / Output
3	VDDIO	Accelerometer Power Supply, Magnetometer Digital Supply
4	NC	Not Internally Connected
5	INTA	Accelerometer Interrupt Active Low and Factory Test (NC/OUT)
6	INTM	Magnetometer Interrupt (NC/Out)
7	VDDM	Magnetometer Analog Supply
8	TM	Magnetometer Factory Test (NC/GND/VDDIO/In)
9	GND	Ground
10	PM	Mag Factory Program (NC/GND/VDDIO)
11	NC	Not Internally Connected
12	SCL	I2C Serial Clock Input

Table 2: Pin Descriptions

3.4 Typical Application Circuit



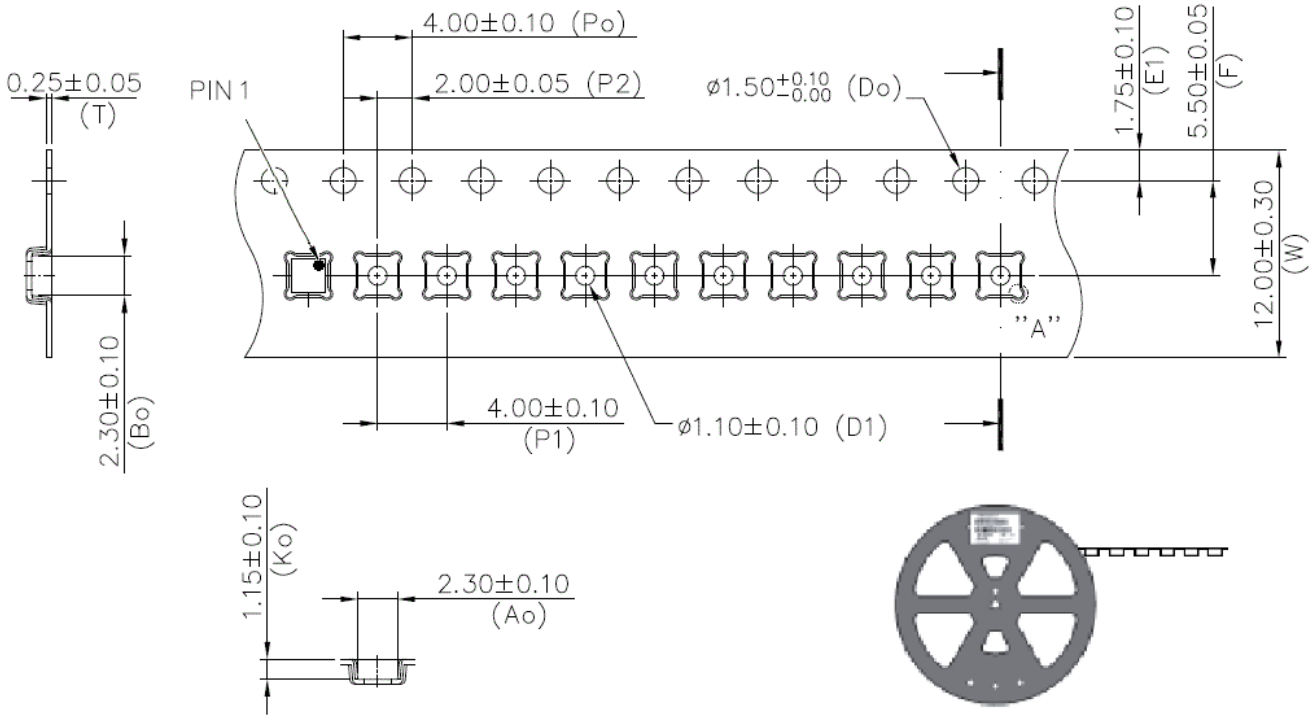
NOTE[1]: Rp are typically 4.7kΩ pullup resistors, per I2C specification. When VDDIO is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTA is defined as open-drain. No pullup is required on INTM.

Figure 6. Typical Application Circuit

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be isolated from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDDM pin.

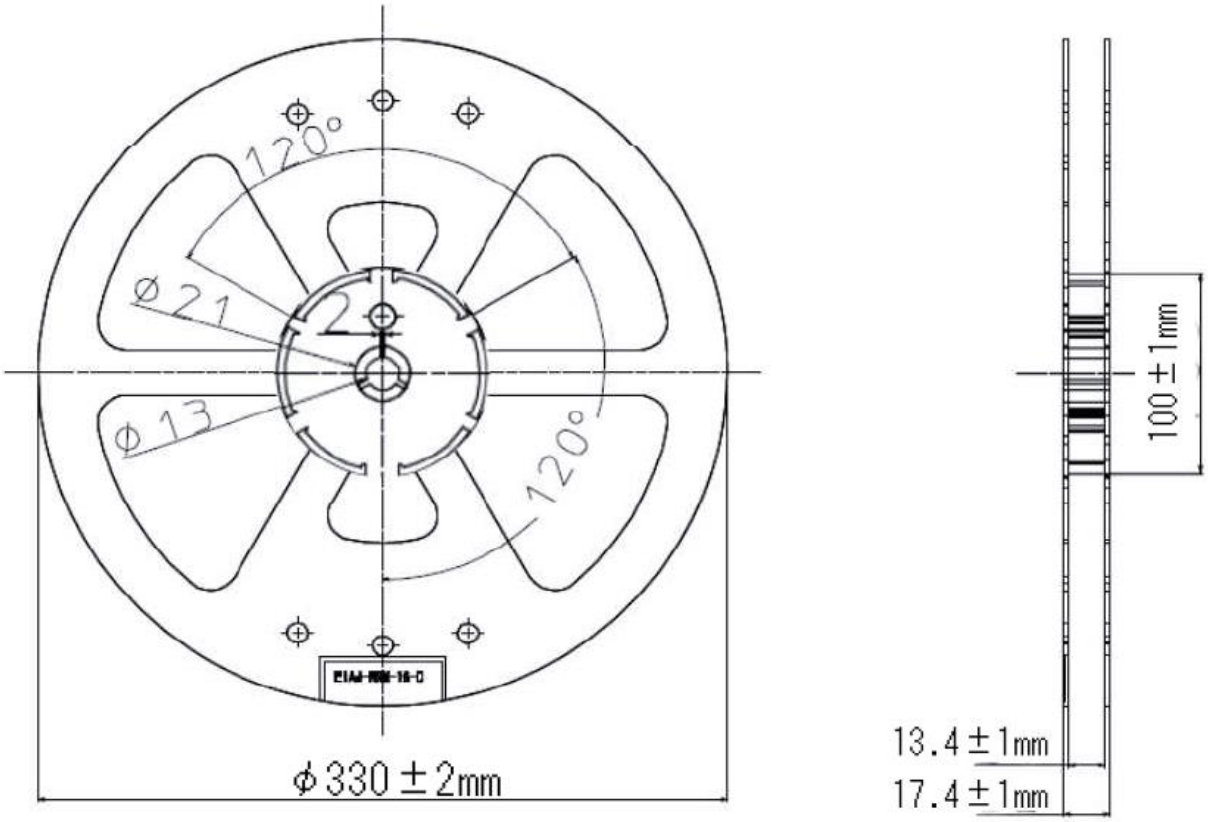
3.5 Tape and Reel

Devices are shipped in reels, in standard cardboard box packaging. See **Figure 7. MC6470 Tape Dimensions** and **Figure 8. MC6470 Reel Dimensions**.



- Dimensions in mm.

Figure 7. MC6470 Tape Dimensions



- Dimensions in mm.

Figure 8. MC6470 Reel Dimensions

4 SPECIFICATIONS

4.1 Absolute Maximum Ratings

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply voltage	Pins VDDM, VDDIO	-0.3 / +3.6	V
Acceleration, any axis, 100 µs	g_{MAX}	10000	g
Magnetic field	H_{MAX}	0.2	T
Storage temperature	T_{STG}	-40 / +125	^{0}C
ESD human body model	HBM	±2000	V
Input voltage to non-power pin	Pins A5, INTA, INTM, PM, SCL, SDA, TM	-0.3 / (VDD + 0.3) or 3.6, whichever is lower	V

Table 3. Absolute Maximum Ratings

4.2 Magnetometer Sensor Characteristics

Test condition: VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Magnetometer Field Range [1]		-2.4		+2.4	mT
Magnetometer Sensitivity [1]			0.15		μT / LSB
Noise	Standard deviation of 100 readings		0.35		μT_{RMS}
Magnetometer Linearity	±2.4mT	-2		+2	% FS
Magnetometer Sample Rate [1]	Programmable	0.5		100	Hz

Table 4. Magnetometer Sensor Characteristics

[1] Values are based on device characterization, not tested in production.

4.3 Accelerometer Sensor Characteristics

Test condition: VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range	Resolution and range set in **OUTCFG: Output Configuration Register**		±2 ±4 ±8 ±16		g
Sensitivity	Depends on settings in **OUTCFG: Output Configuration Register**	8		4096	LSB/g
Sensitivity Temperature Coefficient [2]	-10 ≤ T_{op} ≤ +55 ^{0}C		± 0.025		%/^{0}C
Zero-g Offset			± 40		mg
Zero-g Offset Temperature Coefficient [1]	-10 ≤ T_{op} ≤ +55 ^{0}C		± 1		mg/^{0}C
Noise Density [1]			200		µg/√Hz
Nonlinearity [1]			0.5		% FS
Cross-axis Sensitivity [1]	Between any two axes		2		%

Table 5. Accelerometer Sensor Characteristics

[2] Values are based on device characterization, not tested in production.

4.4 Electrical Characteristics

Test condition: VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDM = VDDIO	VDD	1.7	2.8V	3.6	V
Operating temperature		T_a	-40		+85	^{0}C
Accelerometer Sample Rate Tolerance		T_{clock}	-10		10	%
Standby Current	VDD=2.8V, 25C	I_{dd0}		7		µA
Accelerometer WAKE state supply current	(highly dependent on sample rate)	$I_{dd0.25}$ I_{dd256}		50 130		µA µA
Magnetometer Continuous Measurement Mode	Average (ODR = 10Hz) Average (ODR = 100Hz)			60 600		µA µA
Magnetometer Peak Current Draw	Instantaneous draw only during measurement			2.5		mA
Pad Leakage	Per I/O pad	I_{pad}	-1	0.01	1	µA

Table 6. Device Electrical Characteristics

4.5 I2C Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	V_{IL}	-0.5	0.3*VDD	V
HIGH level input voltage	V_{IH}	0.7*VDD	-	V
Schmitt trigger input hysteresis	V_{hys}	0.05*VDD	-	V
Output voltage, pins INTA, INTM, $I_{ol} \leq 2$ mA	V_{ol} V_{oh}	0 0	0.4 0.9*VDD	V V
Output voltage, pin SDA (open drain), $I_{ol} \leq 1$ mA	V_{ols}	-	0.1*VDD	V
Input current, pins A5, PM, SDA, SCL, TM (input voltage between 0.1*VDD and 0.9*VDD max)	I_i	-10	10	µA
Capacitance, pins SDA, SCL	C_i	-	10	pF

Table 7. I2C Electrical Characteristics

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL to VDDIO should exist.
- Care must be taken to not violate the I2C specification for capacitive loading.
- When VDDIO is not powered and set to 0 V, INTA, INTM, SDA and SCL will be held to VDD plus the forward voltage of the internal static protection diodes, typically about 0.6 V.
- When VDDIO is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.
- Characteristics not tested in production.

4.6 I2C Timing Characteristics

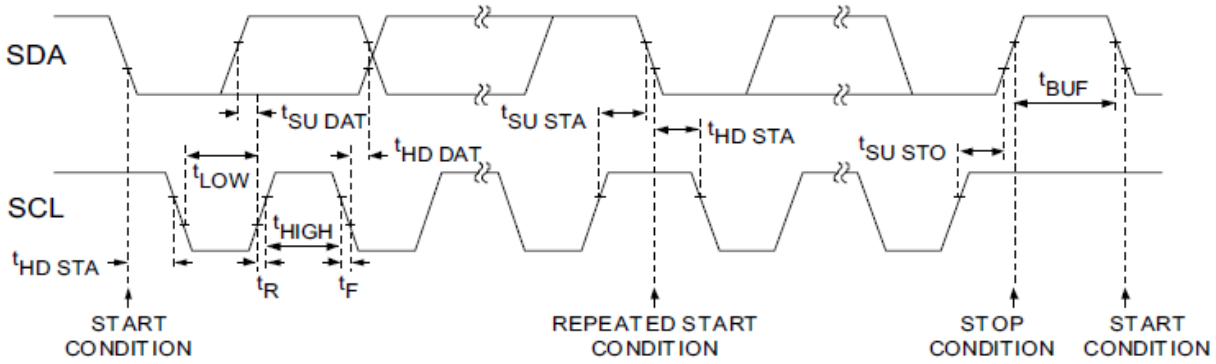


Figure 9. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT(Acc)}$	Data hold time	5	-	-	-	µs
$t_{HD;DAT(Mag)}$	Data hold time	0	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	µs

Table 8. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

4.7 Power Supply Sequence

The timing and sequence requirements of the power supply pins are shown below.

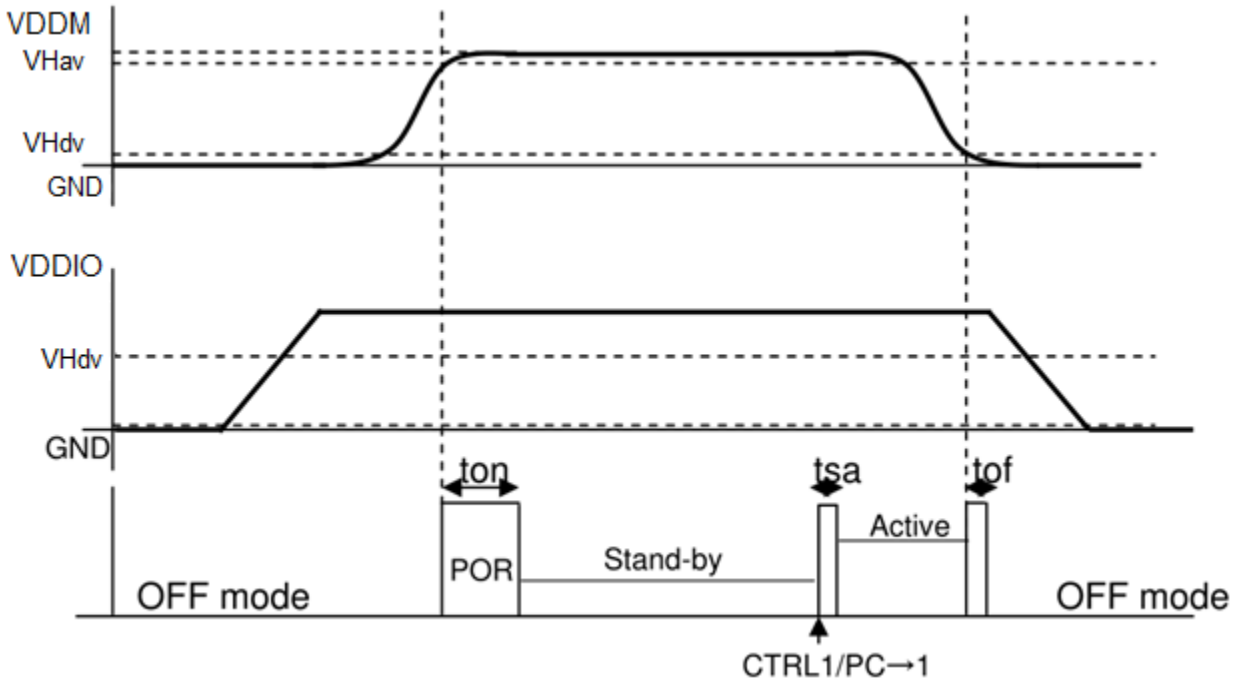


Figure 10 - Power Supply Sequence 1

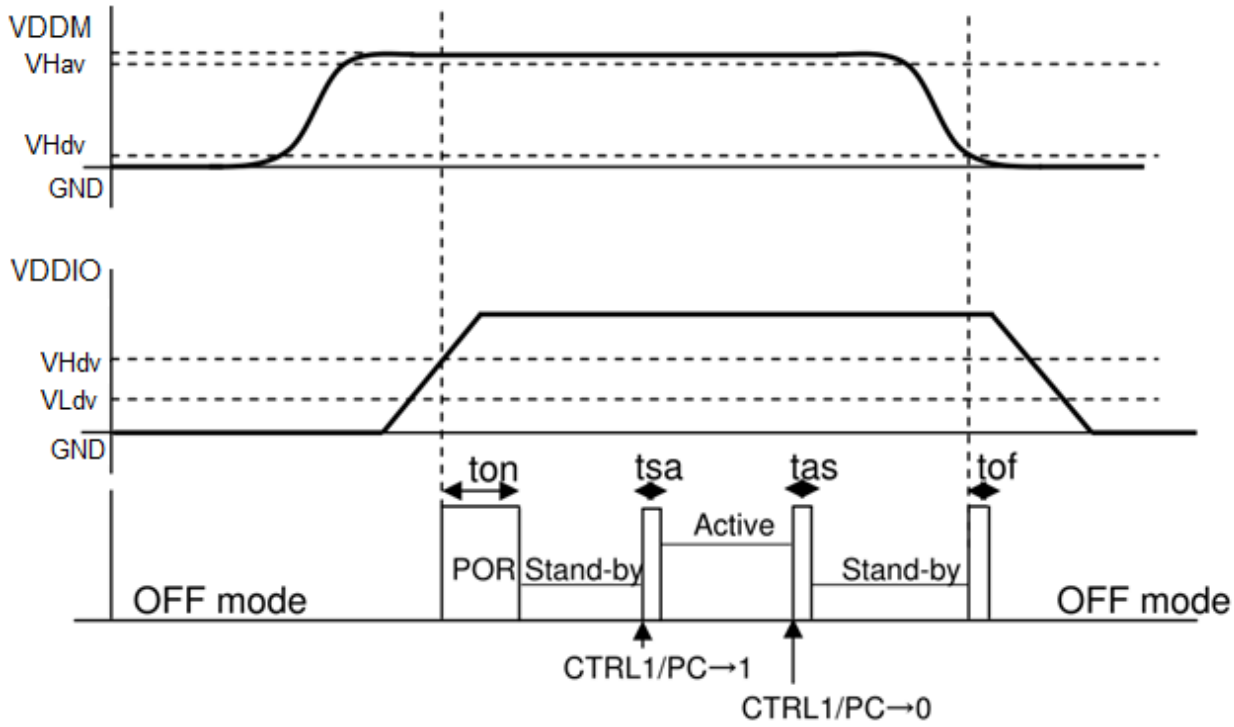


Figure 11 - Power Supply Sequence 2

Parameters on Supply voltage sequence (All Condition)

Transition	Symbol	Typ.	Max.	Unit
OFF→Stand-by	ton	-	3	ms
Stand-by→Active	tsa	-	5	μs
Active→Stand-by	tas	-	5	μs
Active or Stand-by→OFF	tof	-	10	ms

Table 9 - Power Supply Voltage Timing

Parameters on Supply voltage sequence (All Condition)

Characteristics	Symbol	Min.	Max.	Unit
VDDM ON	VHav	1.75	-	V
VDDM OFF	VLav	-	0.17	V
VDDIO ON	VHdv	1.53	-	V
VDDIO OFF	VLdv	-	0.17	V

Table 10 - Power Supply Voltage Levels (for sequencing purposes only)

- There is no limitation in the turn-on timing of the VDDM and the VDDIO voltages.
- Case 1:
  - When the VDDIO voltage turns on initially.
  - After the VDDM voltage has risen (reached VHdv).
  - The rising slope of VDDM must rise (reach 0.9*VDDM) within 1.5 [msec].

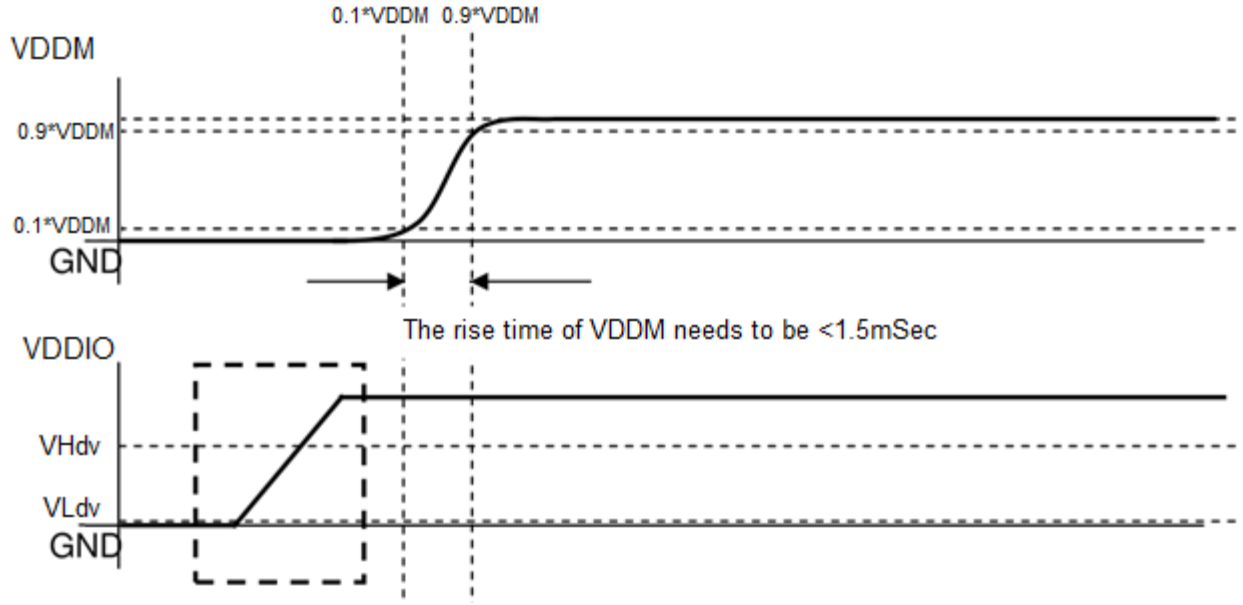


Figure 12 - VDDM and VDDIO Turn-On Timing

5 MAGNETOMETER SUBSECTION

5.1 Magnetometer Operational Modes

The various operational modes of the magnetometer are shown below.

Initialization	Power on reset is performed by turning on the power. All circuits and registers are set to default and the mode is set to stand-by mode automatically by POR. Software reset can be performed by writing to a control register. All registers is reloaded from OTP and the internal compensation table is reloaded.
Self-Test	Self-test confirms the operation of the sensor by register command.
Functional Modes	The sensor has stand-by mode and active mode for power control. There are two states in active mode.
Off mode	The sensor is not active when VDDIO or VDDM is disabled.
Stand-by Mode	Low power state. Stand-by mode can access I2C registers (read / write).
Active Mode	Change from stand-by to active mode by register command to control register.
Force State	Start to measure and output data by register command. Force state is default.
Normal State	Measure sampled magnetometer data by using an internal timer.
Data Ready Function	Occurs when new measured results are updated. The INTM pin can be used to indicate new sample data is available.
Offset Calibration Function	Sensor offset can be canceled by using internal DAC circuit and digital compensation function.
Offset Drift Function	When magnetic field strength drifts, the output data values can be compensated by writing to the offset value registers.
Temperature Measurement Function	Retrieve temperature data from internal temperature sensor. Temperature data is used for internal compensation of output data.
Temperature Compensation Function	Compensate gain, via digital circuitry, by temperature measurement results.

The magnetometer has several states whose primary purpose is power management. A simplified state diagram is shown below.

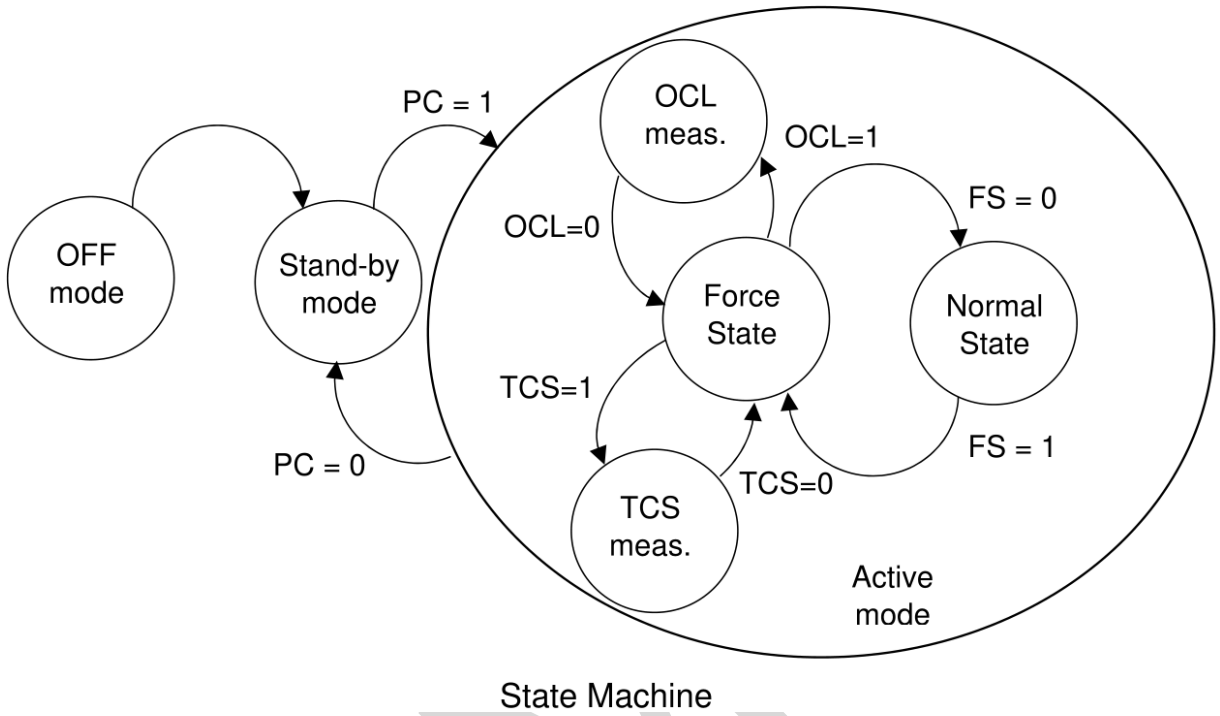


Figure 13. Magnetometer State Diagram

5.2 Initialization

- All internal circuits and all register values are initialized by an internal POR (Power On Reset) circuit after power-on.
- After initialization, the functional mode moves to standby mode automatically.
- The software reset set by the register command SRST=1 sets all register value to defaults and reload the compensation values for internal sensor calculation.

5.2.1 Self-Test

- Self-test can be used to confirm the internal sensor interface and digital logic.
- Self-test is performed by reading the STB register and setting the register
- command CTRL3 STC bit to Hi.
- The following chart shows the procedure to execute self-test.
- Following a properly function self-test operation, the value of response register STB will be set to 0x55.

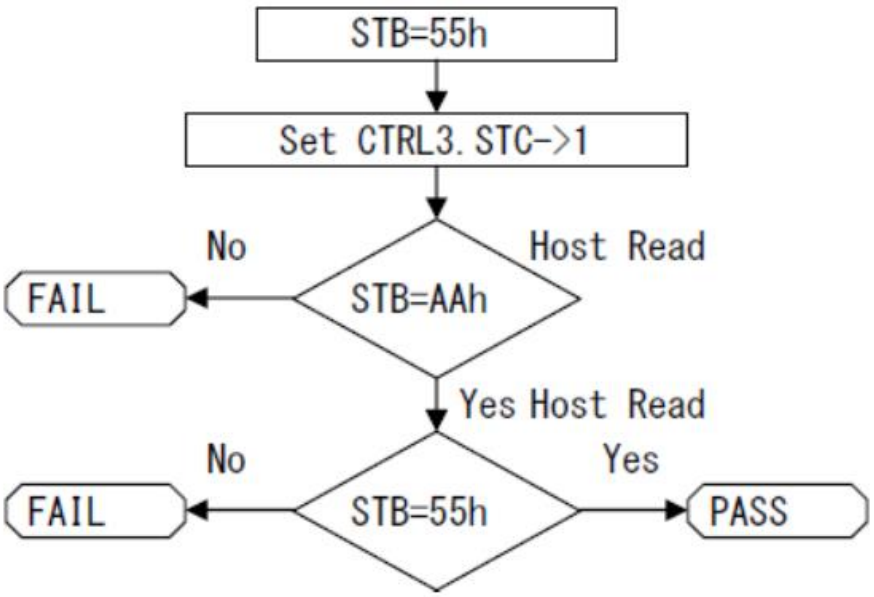


Figure 14 - Self Test Flow Chart

5.3 Modes

5.3.1 OFF mode

The sensor is not active when VDDM or VDDIO is disabled.

5.3.2 Stand-by mode

After loading the POR (Power On Reset), internal state is moved to the standby mode automatically.

Read and Write access function is limited to the following in stand-by mode:

- Write: (CTRL3) FORCE, TCS and STC are disabled
- Read: All resisters can be read.
- Register is changed from the Active mode to the Stand-by mode by setting PC=0 (CNTL1).

5.3.3 Active mode

At active mode, each function can be performed by setting control register 3 (CTRL3). To transfer to active mode, set the PC=1 (CTRL1).

- There are two types of measurement state. One is periodical measurement "Normal state," controlled by inner timer, and the other is "Force state," controlled by register command set by I2C access.
- The measurement state is selectable with FS bit on control register 1 (CTRL1).
- The default of measurement state is the force state (FS=1) after POR or reset running.

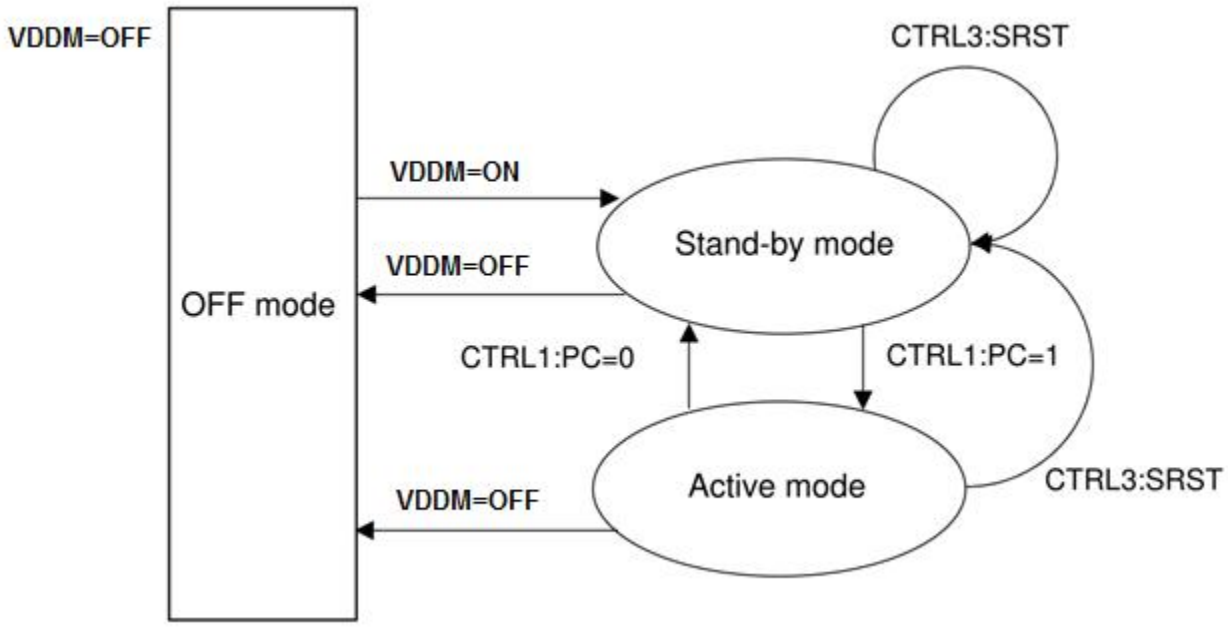


Figure 15 - Transferring Between Modes

5.3.3.1 FORCE STATE

Force State is used for synchronous measurement (selected from register CTRL3, bit FRC). Measurements start after forced register command are written to register via I2C.

- Functional mode changes from Stand-by mode to Active mode by setting register (Control1: bit PC) to "1".
- Force State is set by control register (CNTL1: bit FS) "1".
- Acquired data stored to output register (OUTX, OUTY, OUTZ), and status register (STAT: bit INTM) is set to "1" and output signal (INTM PIN) are set to active.
- Output on external INTM PIN is set by control register (CNTL2).
- During reading data, output register is not updated. After reading is complete, reading data is updated.
- Change of state from Normal to Force is valid after measurement if control register is set during the Active measuring in Normal state.

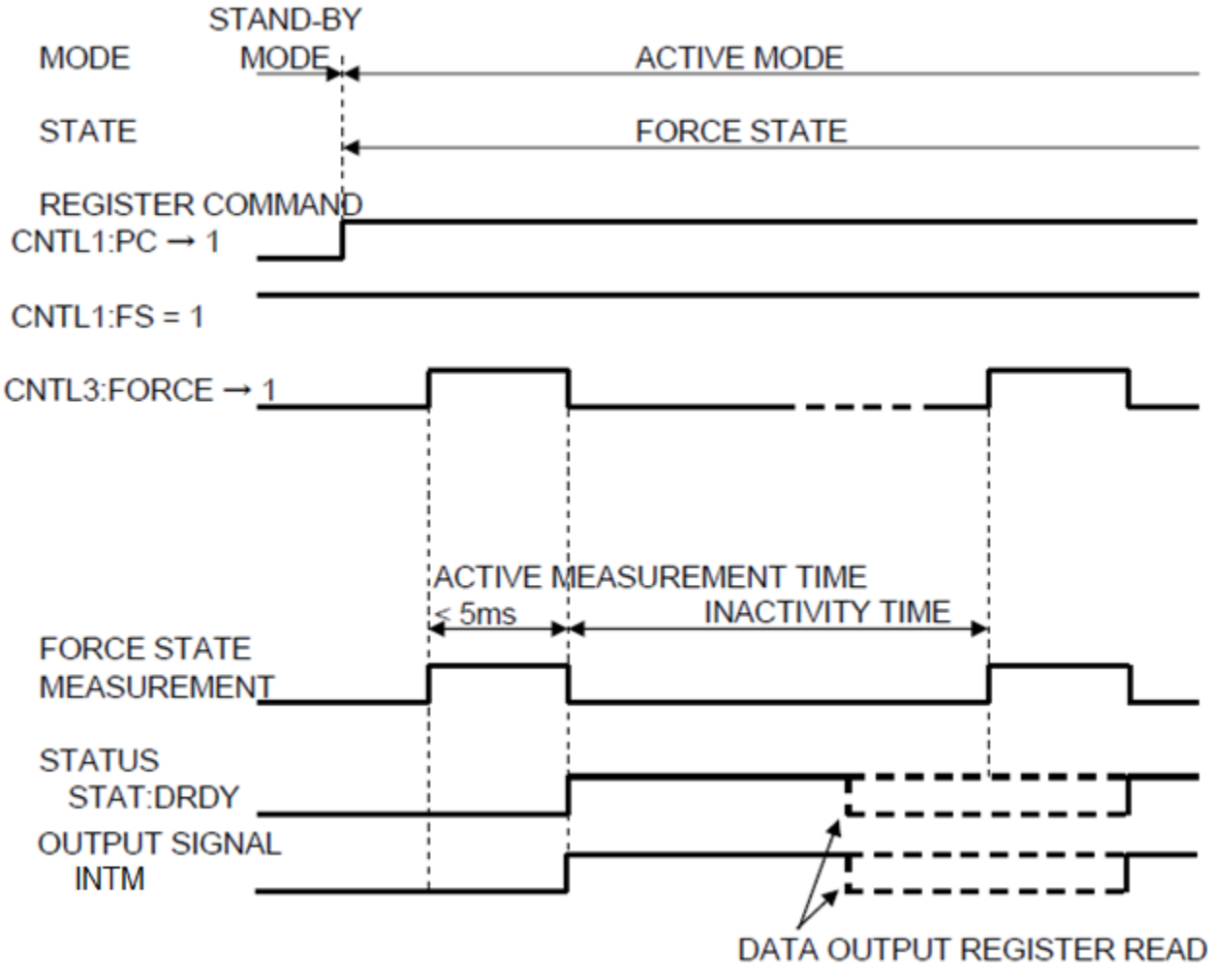


Figure 16 - Measurement Control Timing (Force State)

5.3.3.2 NORMAL STATE

- Normal state is a continuous measurement state, and when Normal state is set by setting “0” to control register (CNTL1: bit FS), a measurement is started.
- Measurement time and interval are managed by an internal clock.
- Functional mode is changed from Stand-by mode to Active mode by setting register (CNTL1: bit PC) to "1".
- Output data rate (ODR) is selectable between 0.5Hz or 100Hz by register (CNTL1: bit ODR).
- Acquired data are stored to register (OUTX, OUTY, OUTZ), status register (STAT: bit DRDY) is set to "1" and output signal INTM are control with (CNTL2:bit DEN).

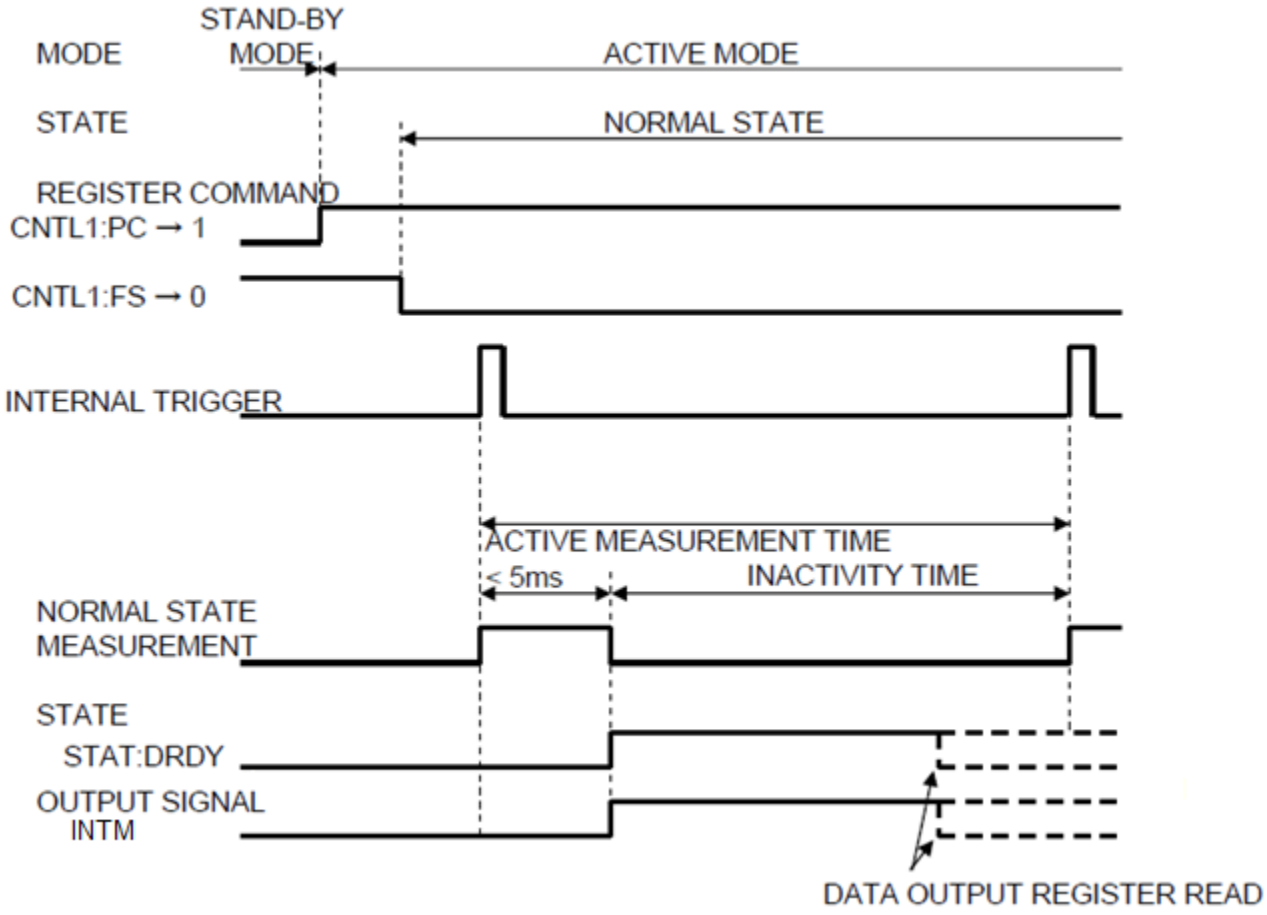


Figure 17 - Measurement Control Timing (Normal State)

5.4 Magnetometer Interrupt Output (INTM pin)

- This function is used to indicate that output sample data has been updated.
- Data ready output is enabled on the INTM PIN, when the sensor data has been updated.
- The status (active / inactive) of the data ready pin can be read via the status register (STAT).
- INTM is changed to inactive after reading data on the output register.
- Conditions of data ready function can be set in the control register (CTRL2).

CNRL2 bit	Bit Name	Default	Condition
4	DEN	0	Output control on INTM PIN 0 = Disable 1 = Enable
3	DRP	1	The polarity setting on INTM PIN 0 = Active Low 1 = Active High

Table 11 - Control Of INTM Interrupt Output Pin

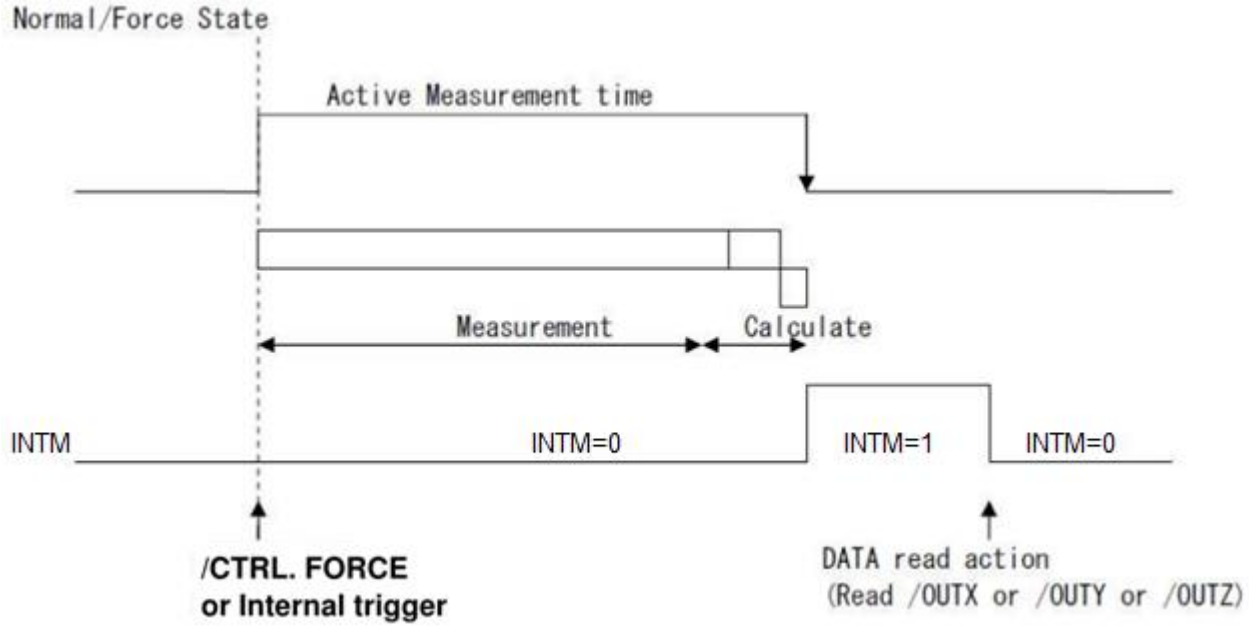


Figure 18 - Data Ready (INTM) Interrupt Function

5.5 Offset Calibration

- This function is enabled when control register (CNTL3:OCL) is set to Hi during the Force State.
- The offset value for inner ADC output is calculated with the measured sensor offset, and then compensation values for the amplitude offset and the digital offset are set automatically.
- The OCL bit is changed to be low after the compensation offset value is updated, and then the status is back to what it was before measurement.

5.6 Offset Drift

- This function can make the digital compensation output that is add with values wrote by the host CPU on the offset drift register (OFFX, OFFY, OFFZ).
- Offset drift values can be set with 15bit signed value.

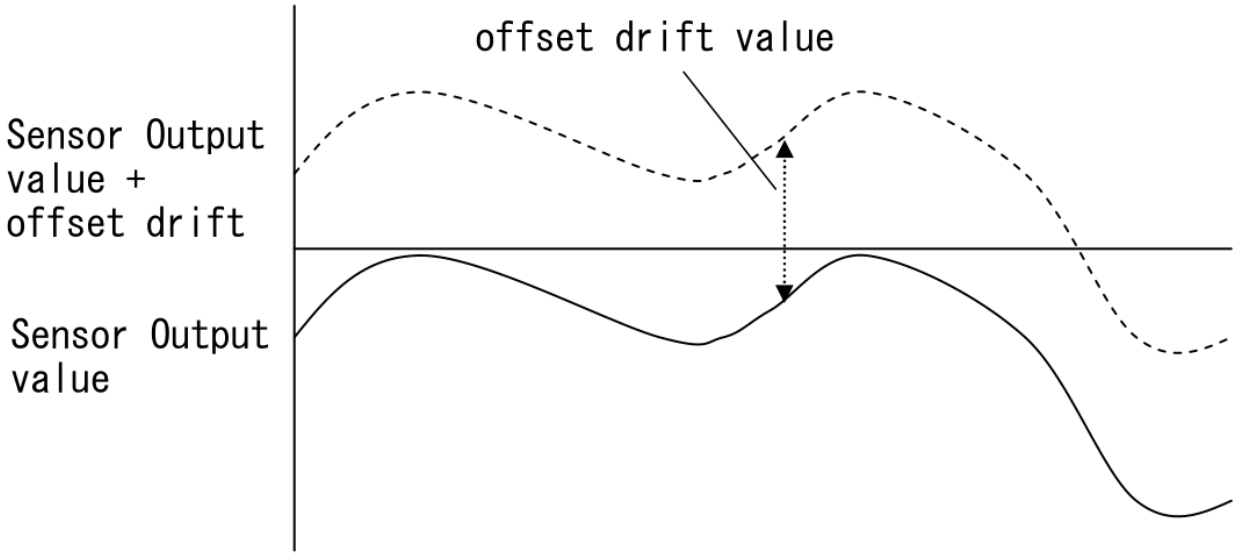


Figure 19 - Magnetometer Offset Drift

5.7 Temperature Measurement and Compensation Function

- The temperature measurement function is executed by setting the register command TCS to "1" while in Force State. After measurement, TCS bit change to "0" and back to what it was before measurement.
- The measurement result is updated in the temperature value register (TEMP).
- Sensor output values are compensated with the temperature value register (TEMP).

6 ACCELEROMETER SUBSECTION

6.1 Accelerometer Operation

The device supports the reading of samples and device status upon interrupt or via polling.

6.1.1 Accelerometer Sensor Sampling

Measurement data is stored in the “extended” registers XOUT_EX, YOUT_EX, and ZOUT_EX. The byte with the lower address of the byte pair is the least significant byte while the byte with the next higher address is the most significant byte. The measurement data is represented as 2’s complement format.

The desired resolution and full scale acceleration range are set in **OUTCFG: Output Configuration Register**.

6.1.2 Accelerometer Offset and Gain Calibration

Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

6.1.3 Accelerometer Tap Detection

The device supports directional tap detection in ±X, ±Y or ±Z. Each axis is independent, although only one direction per axis is supported simultaneously. The threshold, duration, and dead-time of tap detection can be set for each axis, and six flag/status bits are maintained in a status register. The tap hardware uses a second order high-pass filter to detect fast impulse/transition acceleration events. The external interrupt pin can be used to indicate that a tap event has been detected.

6.2 Accelerometer Operational States

The device has two states of operation: STANDBY (the default state after power-up), and WAKE.

The STANDBY state offers the lowest power consumption. In this state, the I2C interface is active and all register reads and writes are allowed. There is no event detection, sampling, or acceleration measurement in the STANDBY state. Internal clocking is halted. Complete access to the register set is allowed in this state, but interrupts cannot be serviced. The device defaults to the STANDBY state following power-up. The time to change states from STANDBY to WAKE is less than 10uSec.

Registers can be written (and therefore resolution, range. thresholds and other settings changed) only when the device is in STANDBY state.

The I2C interface allows write access to all registers only in the STANDBY state. In WAKE state, the only I2C register write access permitted is to the **MODE: Register**. Full read access is allowed in all states.

State	I2C Bus	Description
STANDBY	Device responds to I2C bus (R/W)	Device is powered; Registers can be accessed via I2C. Lowest power state. No interrupt generation, internal clocking disabled. Default power-on state.
WAKE	Device responds to I2C bus (Read)	Continuous sampling and reading of sense data. All registers except the **MODE: Register** are read-only.

Table 12. Operational States

6.3 Accelerometer Operational State Flow

The figure below shows the operational state flow for the device. The device defaults to STANDBY following power-on.

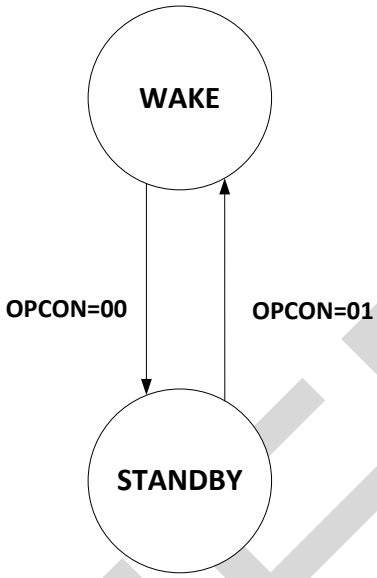


Figure 20. Operational State Flow

The operational state may be forced to a specific state by writing into the OPCON bits, as shown below. Two bits are specified in order to promote software compatibility with other MEMSIC devices. The operational state will stay in the mode specified until changed:

Action	Setting	Effect
Force Wake State	OPCON[1:0] = 01	• Switch to WAKE state and stay there • Continuous sampling
Force Standby State	OPCON[1:0] = 00	• Switch to STANDBY state and stay there • Disable sensor and event sampling

Table 13. Forcing Operational States

6.4 Accelerometer Interrupts

The sensor device utilizes output pin INTA to signal to an external microprocessor that an event has been sensed. The microprocessor would contain an interrupt service routine which would perform certain tasks after receiving this interrupt and reading the associated status bits, perhaps after a sample was made ready. If interrupts are to be used, the microprocessor must set up the registers in the sensor so that when a specific event is detected, the microprocessor would receive the interrupt and the interrupt service routine would be executed. If polling is used there is no need for the interrupt registers to be set up.

For products that will instead use polling, the method of reading sensor data would be slightly different. Instead of receiving an interrupt when an event occurs, the microprocessor must periodically poll the sensor and read status data (the INTA pin is not used). For most applications, this is likely best done at the sensor sampling rate or faster.

Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

6.4.1 Accelerometer Enabling and Clearing Interrupts

The **SR: Status Register** contains the flag bits for the sample acquisition interrupt ACQ_INT. The **INTEN: Interrupt Enable Register** determines if a flag event generates interrupts.

The flags (and interrupts) are cleared and rearmed each time the **SR: Status Register** is read.

When an event is detected, it is masked with a flag bit in the **INTEN: Interrupt Enable Register**, and then the corresponding status bit is set in the **SR: Status Register**.

The polarity and driving mode of the external interrupt signal may be chosen by setting the IPP and IAH bits in the **MODE: Register**.

6.4.2 Accelerometer ACQ_INT Interrupt

The ACQ_INT flag bit in the **SR: Status Register** is always active. This bit is cleared when it is read. When a sample has been produced, an interrupt will be generated only if the ACQ_INT_EN bit in the **INTEN: Interrupt Enable Register** is active. Note that the frequency of this ACQ_INT bit being set active is always the same as the sample rate.

6.5 Accelerometer Continuous Sampling

The device has the ability to read all sampled readings in a continuous sampling fashion. The device always updates the XOUT, YOUT, and ZOUT registers at the chosen ODR.

An optional interrupt can be generated each time the sample registers have been updated (ACQ_INT interrupt bit in the **INTEN: Interrupt Enable Register**).

6.6 Accelerometer Watchdog Timer

When enabled (see **MODE: Register**), the I2C watchdog timer prevents bus stall conditions in cases where the master does not provide enough clocks to the slave to complete a read cycle.

During a read cycle, the slave that is actively driving the bus (SDA pin) will not release the bus until 9 SCL clock edges are detected. While the SDA pin is held low by a slave open-drain output, any other I2C devices attached to the sample bus will be unable to communicate. If the slave does not see 9 SCL clocks from the master within the timeout period, the slave will assume a system problem has occurred

and so the I2C circuitry will be reset, the SDA pin released and the sensor made ready for additional I2C commands.

No other changes to registers are made.

When enabled, the I2C watchdog timer does not resolve why the master did not provide enough clocks to complete a read cycle, but it does prevent a slave from holding the bus indefinitely.

When enabled, the timeout period is about 200mSec.

When an I2C watchdog timer event is triggered, the I2C_WDT bit in register will be set active by the Watchdog timer hardware. External software can detect this status by noticing this bit is active. The act of reading register 0x04 will clears the status.

7 I2C INTERFACE

The I2C slave interface operates at a maximum speed of 400 kHz. The device has a single set of I2C signals connecting to independent I2C interfaces. The SDA (data) signal is an open-drain, bi-directional pin. The SCL (clock) signal is an input pin. SCL and SDA each require an external pull-up resistor.

The device always operates as an I2C slave on both magnetometer and accelerometer I2C interfaces.

An external I2C master must initiate all communication and data transfers and generate the SCL clock that synchronizes the data transfer.

7.1 Accelerometer I2C Interface

The accelerometer I2C device address depends upon the state of the A5 pin during power-up as shown in the table below. The I2C device default addresses for the magnetic sensor is 0x0C.

7-bit Device ID	8-bit Address – Write	8-bit Address – Read	Pin A5 level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

Table 14. Accelerometer I2C Address Selection

An optional I2C watchdog timer reset can be enabled to prevent bus stall conditions. When enabled, the accelerometer I2C circuitry will reset itself if the master takes too long to issue clocks to the sensor during a read cycle (i.e. if there is a gap in SCL clocks of more than about 200mSec). A status bit can be read to observe if this condition has occurred.

The accelerometer I2C interface remains active as long as power is applied to the VDDIO pin.

In the accelerometer, the device responds to I2C read and write cycles when it is in STANDBY state, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY state, but in WAKE state, only the **MODE: Register** can be modified. Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

The accelerometer requires a Stop bit between I2C transactions. Refer to the I2C specification for a detailed discussion of the protocol.

7.2 Magnetometer I2C Interface

The acceleration sensor supports Standard mode and Fast mode.

The magnetic sensor supports Standard mode, Fast mode, Fast mode Plus and Hi speed mode.

The magnetic sensor can seamlessly change from Fast mode to Hi speed mode using the master code (00001XXX).

The magnetic sensor supports multiple Read and Write mode.

The I2C clock stretch function is not supported.

7.3 I2C Message Format

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK. For example, assuming pin A5 was low upon device startup, this means from an 8-bit point of view of an external I2C master, writes should be written to address 0x98 (for accelerometer) and reads will occur by reading address 0x99 (for accelerometer).

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

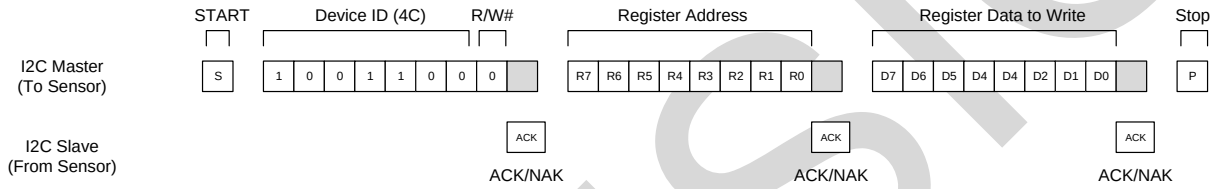


Figure 21. I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W# = 0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.

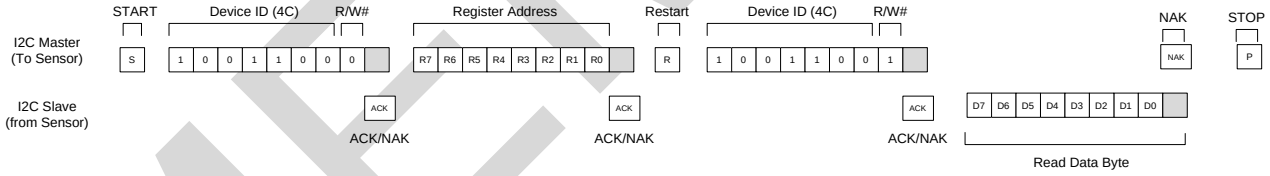


Figure 22. I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

8 MAGNETOMETER REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

Sensor output values are signed integer (2's complement) presentation and little Endian order

The following table summarizes the registers in Magnetometer.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00-0B	---	---	---	---	---	---	---	---	---	00
0C	SelfTest response	STB[7:0]								55
0D	More Info version	0	0	0	1	0	0	0	1	11
0E	More Info	0	0	0	1	0	1	0	1	15
0F	Who I am	0	1	0	0	1	0	0	1	49
10	Output X LSB	OUTX[7:0]								00
11	Output X MSB	OUTX[15:8]								00
12	Output Y LSB	OUTY[7:0]								00
13	Output Y MSB	OUTY[15:8]								00
14	Output Z LSB	OUTZ[7:0]								00
15	Output Z MSB	OUTZ[15:8]								00
16-17	---	---	---	---	---	---	---	---	---	00
18	Status	---	DRDY	DOR	---	---	FFU	TRDY	ORDY	00
19	(TBD)	---	---	---	---	FP				00
1A	---	---	---	---	---	---	---	---	---	00
1B	Control1	PC	---	---	ODR[1:0]		---	FS	---	0A
1C	Control2	AVG	FCO	AOR	FF	DEN	DRP	DTS	DOS	04
1D	Control3	SRST	FORCE	---	STC	---	---	TCS	OCL	00
1E	Control4	MMD		---	RS	AS	---	---	---	80
1F	---	---	---	---	---	---	---	---	---	0
20	Offset X LSB	OFFX[7:0]								00
21	Offset X MSB	---	OFFX[14:8]							00
22	Offset Y LSB	OFFY[7:0]								00
23	Offset Y MSB	---	OFFY[14:8]							00
24	Offset Z LSB	OFFZ[7:0]								00
25	Offset Z MSB	---	OFFZ[14:8]							00
26	ITHR_L	ITHR_L								00
27	ITHR_H	---	---	ITHR_H						00
28-2F,30	---	---	---	---	---	---	---	---	---	00
31	Temperature value	TEMP[7:0]								19
32-5F	---	---	---	---	---	---	---	---	---	00

Table 15. Magnetometer Register Summary

8.1 Magnetometer Registers

Self Test Response Register (STB)

Address : 0Ch, Self Test Response (Read Only)

Bit	Name	Description
7:0	STB 7:0	Self test starts by STC bit (CNTL3 register). AAh is stored when CNTL3: bit STC sets to 1. 55h is stored after STB register is read.

Information Registers

Address : 0Dh, More Info version (Read Only)

Bit	Name	Description
7:0	INFO1 7:0	Information Value1 (11h)

Address : 0Eh, More Info (Read Only)

Bit	Name	Description
7:0	INFO2 7:0	Information Value2 (15h)

Address : 0Fh, Who Am I Value (Read Only)

Bit	Name	Description
7:0	WIA 7:0	Identify byte (49h)

Output Data Register (OUTX, OUTY, OUTZ)
- 14bit integer and 1FFFh (8191d) ~ E000h (-8192d)

Address : 10h, X-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTX 7:0	X-axis Output Data, Signed Integer.

Address : 11h, X-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTX 14:8	X-axis Output Data, Signed Integer.

Address : 12h, Y-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTY 7:0	Y-axis Output Data, Signed Integer.

Address : 13h, Y-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTY 14:8	Y-axis Output Data, Signed Integer.

Address : 14h, Z-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTZ 7:0	Z-axis Output Data, Signed Integer.

Address : 15h, Z-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTZ 14:8	Z-axis Output Data, Signed Integer.

Status Register (STAT)

Address : 18h, Status (Read Only)

Bit	Name	Description
7	X	Not Used
6	DRDY	Data Ready Detection 0 = Not Detected, 1 = Detected
5	DOR	Data Overrun Detection 0 = Not Detected, 1 = Detected Note: if Read Output Data Register.
4:3	X	Not Used
2	FFU	Must be use Default setting. 0 = (Default)
1	TRDY	Must be use Default setting. 0 = (Default)
0	ORDY	Must be use Default setting. 0 = (Default)

NOTE: SOFTWARE MUST ALWAYS WRITE '0' TO BITS 0, 1 AND 2.

Control 1 Register (CTRL1)

Address : 1Bh, Control 1 (Write/Read)

Bit	Name	Description
7	PC	Power Mode Control 0 = Stand-by Mode (Default), 1 = Active Mode
6:5	X	Not Used (Read Only)
4:3	ODR 1:0	Output Data Rate Control in Normal State 00 = 0.5 Hz 01 = 10Hz (Default) 10 = 20Hz 11 = 100Hz
2	X	Not Used (Read Only)
1	FS	State Control in Active Mode 0 = Normal State 1 = Force State (Default)
0	X	Not Used (Read Only)

Control 2 Register (CTRL2)

- When a CTRL2 register value was changed during the measurement, The contents of the change are reflected after measurement.

Address : 1Ch, Control 2 (Write/Read)

Bit	Name	Description
7	AVG	Must be use Default setting. 0 = (Default) ※
6	FCO	Must be use Default setting. 0 = (Default) ※
5	AOR	Must be use Default setting. 0 = (Default) ※
4	FF	Must be use Default setting. 0 = (Default) ※
3	—	
2	—	
1	DTS	Must be use Default setting. 0 = (Default) ※
0	DOS	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

Control 3 Register (CTRL3)

- Bit control at the same time is prohibited.
- Priority of this register is MSB.

Address : 1Dh, Control 3 (Write/Read)

Bit	Name	Description
7	SRST	Soft Reset Control Enable 0 = No Action (Default), 1 = Soft Reset Note: return to zero after soft reset.
6	FRC	Start to Measure in Force State 0 = No Action (Default), 1 = Measurement Start Note: return to zero after measurement.
5	X	Not Used (Read Only)
4	STC	Self Test Control Enable 0 = No Action (Default) 1 = Set parameters to Self Test Response (STB) register. Note: return to zero immediately.
3:2	X	Not Used (Read Only)
1	TCS	Start to Measure Temperature in Active Mode 0 = No Action (Default), 1 = Measurement Start
0	OCL	Start to Calibrate Offset in Active Mode 0 = No Action (Default), 1 = Action

Control 4 Register (CTRL4)

- When a CTRL4 register value was changed during the measurement,
  The contents of the change are reflected after measurement.

Address : 1Eh, Control 4 (Write/Read)

Bit	Name	Description
7:6	MMD	Must be use Default setting. 10 = (Default) ※
5	X	Not Used (Read Only)
4	RS	Set Dynamic range of output data. 0 = 14 bit signed value (-8192 to +8191) (Default) 1 = 15 bit signed value (-16384 to +16383)
3	AS	Must be use Default setting. 0 = (Default) ※
2:0	X	Not Used (Read Only)

※. The change of this bit is prohibited.

Offset Drift Value Register (OFFX, OFFY, OFFZ)

- Data is 14bit integer and 1FFFh (8191d) ~ E000h (-8192d)

Address : 20h, 14 bits X-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFX 7:0	X-axis Offset Drift Value, Signed Integer.

Address : 21h, 14 bits X-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFX 13:0	X-axis Offset Drift Value, Signed Integer.

Address : 22h, 14 bits Y-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFY 7:0	Y-axis Offset Drift Value, Signed Integer.

Address : 23h, 14 bits Y-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFY 13:8	Y-axis Offset Drift Value, Signed Integer.

Address : 24h, 14 bits Z-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFZ 7:0	Z-axis Offset Drift Value, Signed Integer.

Address : 25h, 14 bits Z-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFZ 13:8	Z-axis Offset Drift Value, Signed Integer.

Temperature Data Register (TEMP)

- Temperature measurement is performed by setting register command (CNTL3 : bit TCS) when in the active mode
- Result is stored to temperature register (TEMP)
- Sensor output value are compensated with the temperature value stored TEMP register.

Address : 31h, Temperature Data (Read Only)

Bit	Name	Description
7:0	TEMP7:0	Temperature Data, Signed Integer. LSB = 1℃ 1000 0000 = -128℃ 0000 0000 = 0℃ 0111 1111 = 127℃

9 ACCELEROMETER REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

9.1 Register Summary

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[3]
0x00-0x02		RESERVED[4]										
0x03	SR	**Status Register**	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R
0x04	OPSTAT	**Operational Device Status Register**	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R
0x05		RESERVED										
0x06	INTEN	**Interrupt Enable Register**	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W
0x07	MODE	**Mode Register**	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0[5]	OPCON [1]	OPCON [0]	0x00	W
0x08	SRTFR	**Sample Rate and Tap Feature Register**	TAP_LATCH	FLIP_TAPZ	FLIP_TAPY	FLIP_TAPX	RATE[3]	RATE[2]	RATE[2]	RATE[0]	0x00	W
0x09	TAPEN	**Tap Control Register**	TAP_EN	THRDUR	TAPZNEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W
0x0A	TTTRX	**X Tap Duration and Threshold Register**	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	0x00	W
0x0B	TTTRY	**Y Tap Duration and Threshold Register**	TTTRY[7]	TTTRY[6]	TTTRY[5]	TTTRY[4]	TTTRY[3]	TTTRY[2]	TTTRY[1]	TTTRY[0]	0x00	W
0x0C	TTTRZ	**Z Tap Duration and Threshold Register**	TTTRZ[7]	TTTRZ[6]	TTTRZ[5]	TTTRZ[4]	TTTRZ[3]	TTTRZ[2]	TTTRZ[1]	TTTRZ[0]	0x00	W
0x0D	XOUT_EX_L	**XOUT Extended Register**	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	**XOUT Extended Register**	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	**YOUT Extended Register**	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	**YOUT Extended Register**	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	**ZOUT Extended Register**	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	**ZOUT Extended Register**	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R
0x13-0x1F		RESERVED										
0x20	OUTCFG	**Output Configuration Register**	0[5]	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W
0x21	XOFFL	**X-Offset LSB Register**	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	**X-Offset MSB Register**	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x23	YOFFL	**Y-Offset LSB Register**	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	**Y-Offset MSB Register**	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	**Z-Offset LSB Register**	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	**Z-Offset MSB Register**	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[3]
0x27	XGAIN	**X Gain Register**	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x28	YGAIN	**Y Gain Register**	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	**Z Gain Register**	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A-0x3A		RESERVED										
0x3B	PCODE	**Product Code Register**	0	0	0	0	*[6]	*[6]	*[6]	0	Per chip	R
0x3C to 0x3F		RESERVED										

Table 16. Register Summary[7]

[3] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.
[4] Registers designated as 'RESERVED' should not be accessed by software.
[5] Software must always write a zero '0' to this bit.
[6] Bits denoted with '*' might be any value, set by the factory. Software should ignore these bits.
[7] No registers are updated with new event status or samples while a I2C cycle is in process.

9.2 SR: Status Register

This register contains the flag/event bits for tap detection and sample acquisition. The TAP bits will only transition if the corresponding enable bit has been set in register 0x09, the TAP control register. Each read to this register will clear the latched event(s) and re-arm the flag for the next event.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x03	TAPR	Tap Status Register	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R

TAP_XP	Positive X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_XN	Negative X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YP	Positive Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YN	Negative Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZP	Positive Z-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZN	Negative Z-axis TAP detected, flag is set in polling mode or interrupt mode.
ACQ_INT	Sample has been acquired, flag bit is set in polling mode or interrupt mode. This bit cannot be disabled and is always set be hardware when a sample is ready. The host must poll at the sample rate or faster to see this bit transition.

Table 17. SR Status Register

9.3 OPSTAT: Device Status Register

The device status register reports various conditions of the sensor circuitry.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x04	OPSTAT	Operational Device Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R

OPSTAT[1:0]	Sampling State Register Status, Wait State Register Status 00: Device is in STANDBY state, no sampling 01: Device is in WAKE state, sampling at set sample rate 10: Reserved 11: Reserved
I2C_WDT	I2C watchdog timeout 0: No watchdog event detected 1: Watchdog event has been detected by hardware, I2C slave state machine reset to idle. This flag is cleared by reading this register.
OTPA	One-time Programming (OTP) activity status 0: Internal memory is idle and the device is ready for use 1: Internal memory is active and the device is not yet ready for use

Table 18. OPSTAT Device Status Register

9.4 INTEN: Interrupt Enable Register

The interrupt enable register allows the flag bits for specific TAP and sample events to also trigger a transition of the external INTA pin. This is the only effect these bits have as the flag bits will be set/cleared in the **SR: Status Register** regardless of which interrupts are enabled in this register.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W

TIXPEN	Positive X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIXNEN	Negative X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIYPEN	Positive Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIYNEN	Negative Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIZPEN	Positive Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIZNEN	Negative Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
ACQ_INT_EN	Generate Interrupt 0: Disable automatic interrupt on INTA pad after each sample (default). 1: Enable automatic interrupt on INTA pad after each sample.

Table 19. INTEN Interrupt Enable Register Settings

9.5 MODE: Register

The MODE register controls the active operating state of the device. This register can be written from either operational state (STANDBY or WAKE).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0*	OPCON [1]	OPCON [0]	0x00	W

NOTE*: Software must always write a zero '0' to Bit 2.

OPCON [1:0]	00: STANDBY state (default)	Set Device Operational State. WAKE or STANDBY
	01: WAKE state	
	10: Reserved	
	11: Reserved	
I2C_WDT_NEG	0: I2C watchdog timer for negative SCL stalls disabled (default) 1: I2C watchdog timer for negative SCL stalls enabled	WDT for negative SCL stalls
I2C_WDT_POS	0: I2C watchdog timer for positive SCL stalls disabled (default) 1: I2C watchdog timer for positive SCL stalls enabled	WDT for positive SCL stalls
IPP	0: Interrupt pin INTA is open drain (default) and requires an external pull-up to VDDIO.	Interrupt Push Pull
	1: Interrupt pin INTA is push-pull. No external pull-up resistor should be installed.	
IAH	0: Interrupt pin INTA is active low (default)	Interrupt Active High
	1: Interrupt pin INTA is active high	

Table 20. MODE Register Functionality

9.6 SRTFR: Sample Rate and Tap Feature Register

This register sets the sampling output data rate (ODR) for sensor. The upper 4 bit control functions related to tap hardware. The lower 4 bits control the rate, as shown in the table below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x08	SRTFR	Sample Rate and Tap Feature Register	TAP_LATCH	FLIP_TAPZ	FLIP_TAPY	FLIP_TAPX	RATE[3]	RATE[2]	RATE[1]	RATE[0]	0x00	W

RATE[3:0]	0000: 32 Hz (default) 0001: 16 Hz 0010: 8 Hz 0011: 4 Hz 0100: 2 Hz 0101: 1 Hz 0110: 0.5 Hz 0111: 0.25 Hz 1000: 64 Hz 1001: 128 Hz 1010: 256 Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
FLIP_TAPX	0: X positive and X negative tap are not switched (default) 1: X positive and X negative tap are switched
FLIP_TAPY	0: Y positive and Y negative tap are not switched (default) 1: Y positive and Y negative tap are switched
FLIP_TAPZ	0: Z positive and Z negative tap are not switched (default) 1: Z positive and Z negative tap are switched
TAP_LATCH	0: Multiple TAPs (of those which are enabled) are detected and latched (default) 1: First TAP detected (e.g. of those enabled) is latched, all others ignored until serviced by reading register 0x03.

Table 21. SRTFR Register Functionality

9.7 TAPEN: Tap Control Register

This register allows the enabling and disabling of tap detection for axes and direction. Bit 7 disables tap detection completely. Bit 6, switches the feature controlled by registers 0xA, 0xB, and 0xC. When bit 6 is '0', the tap duration and quiet parameters are accessed in 0xA to 0xC, and when '1' the tap detection threshold is accessed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x09	TAPEN	Tap Control Register	TAP_EN	THRDUR	TAPZNEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W

TAPXPEN	0: Disable positive tap detection on X-axis (default) 1: Enable positive tap detection on X-axis
TAPXNEN	0: Disable negative tap detection on X-axis (default) 1: Enable negative tap detection on X-axis
TAPYPEN	0: Disable positive tap detection on Y-axis (default) 1: Enable positive tap detection on Y-axis
TAPYNEN	0: Disable negative tap detection on Y-axis (default) 1: Enable negative tap detection on Y-axis
TAPZPEN	0: Disable positive tap detection on Z-axis (default) 1: Enable positive tap detection on Z-axis
TAPZNEN	0: Disable negative tap detection on Z-axis (default) 1: Enable negative tap detection on Z-axis
THRDUR	0: Registers 0xA, 0xB, 0xC point to tap duration and quiet period (default) 1: Registers 0xA, 0xB, 0xC point to tap threshold settings. See description of TTTRX, TTTRY and TTTRZ.
TAP_EN	0: All tap detection is disabled, regardless of bits [5:0] (default) 1: Tap detection is enabled, individual enables control detection (bits 5-1)

Table 22. TAPEN Register Settings

9.8 TTTRX,TTTRY, TTTRZ: X, Y and Z Tap Duration and Threshold Registers

These 3 registers allow control of both the tap duration settings and tap threshold settings, depending upon the setting of the THRDUR bit (bit 6) in the TAPEN register (0x09).

When THRDUR=0, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Quiet-Duration	TAP X Duration Register	TAP_X_QUIET[3]	TAP_X_QUIET[2]	TAP_X_QUIET[1]	TAP_X_QUIET[0]	TAP_X_DUR[3]	TAP_X_DUR[2]	TAP_X_DUR[1]	TAP_X_DUR[0]	0x00	W
0x0B	Tap Y Quiet-Duration	TAP Y Duration Register	TAP_Y_QUIET[3]	TAP_Y_QUIET[2]	TAP_Y_QUIET[1]	TAP_Y_QUIET[0]	TAP_Y_DUR[3]	TAP_Y_DUR[2]	TAP_Y_DUR[1]	TAP_Y_DUR[0]	0x00	W
0x0C	Tap Z Quiet-Duration	TAP Z Duration Register	TAP_Z_QUIET[3]	TAP_Z_QUIET[2]	TAP_Z_QUIET[1]	TAP_Z_QUIET[0]	TAP_Z_DUR[3]	TAP_Z_DUR[2]	TAP_Z_DUR[1]	TAP_Z_DUR[0]	0x00	W

When THRDUR=1, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Thresh	TAP X Threshold Register	TAP_X_TH[7]	TAP_X_TH[6]	TAP_X_TH[5]	TAP_X_TH[4]	TAP_X_TH[3]	TAP_X_TH[2]	TAP_X_TH[1]	TAP_X_TH[0]	0x00	W
0x0B	Tap Y Thresh	TAP Y Threshold Register	TAP_Y_TH[7]	TAP_Y_TH[6]	TAP_Y_TH[5]	TAP_Y_TH[4]	TAP_Y_TH[3]	TAP_Y_TH[2]	TAP_Y_TH[1]	TAP_Y_TH[0]	0x00	W
0x0C	Tap Z Thresh	TAP Z Threshold Register	TAP_Z_TH[7]	TAP_Z_TH[6]	TAP_Z_TH[5]	TAP_Z_TH[4]	TAP_Z_TH[3]	TAP_Z_TH[2]	TAP_Z_TH[1]	TAP_Z_TH[0]	0x00	W

TAP_X_DUR[3:0] TAP_Y_DUR[3:0] TAP_Z_DUR[3:0]	This 4-bit value (0 to 15) sets the maximum number of samples an event must qualify as a tap before it is rejected. For example, if the value is 4, a fast acceleration event which exceeded the threshold for more than 4 consecutive samples would not trigger a tap event.
TAP_X_QUIET[3:0] TAP_Y_QUIET[3:0] TAP_Z_QUIET[3:0]	This 4-bit value (0 to 15) sets the number of samples to be ignored after successful tap detection. Detection is rearmed after the specific number of samples has passed.
TAP_X_TH[7:0] TAP_Y_TH[7:0] TAP_Z_TH[7:0]	This 8-bit unsigned value sets the minimum magnitude a snap event must reach before a tap is considered detected. Setting this parameter to a higher value will effectively reject all but the largest acceleration events as tap. Some experimentation in the final form-factor may be needed to find an appropriate setting for a particular product.

Table 23. TTTRX, TTTRY and TTTRZ Register Settings

9.9 XOUT_EX, YOUT_EX & ZOUT_EX: X, Y, Z-Axis Acceleration Registers

The measurements from sensors for the 3-axes are available in these 3 registers. The most-significant bit of the value is the sign bit, and is sign extended to the higher bits. Note that all 3 axes are sampled and updated simultaneously. If an I2C burst read operation reads past register address 0x12 the internal address pointer “wraps” to address 0x03 and the contents of the **SR: Status Register** are returned. This allows application software to burst read the contents of the six extended registers and relevant device state registers in a single I2C read cycle.

Once an I2C start bit has been recognized by the sensor, registers will not be updated until an I2C stop bit has occurred. Therefore, if software desires to read the low and high byte registers ‘atomically’, knowing that the values have not been changed, it should do so by issuing a start bit, reading one register, then reading the other register then issuing a stop bit. Note that all 6 registers may be read in one burst with the same effect.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R

Table 24. Extended Accelerometer Registers

9.10 OUTCFG: Output Configuration Register

This register can be used to set the range and resolution of the accelerometer measurements.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	OUTCFG	Output Configuration Register	0*	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W

NOTE*: Software must always write a zero '0' to Bit 7.

RES[2:0]	Accelerometer g Resolution 000: Select 6-bits for accelerometer measurements (Default) 001: Select 7-bit for accelerometer measurements 010: Select 8-bit for accelerometer measurements 011: Select 10-bit for accelerometer measurements 100: Select 12-bit for accelerometer measurements 101: Select 14-bit for accelerometer measurements 110: Reserved 111: Reserved
RANGE[2:0]	Accelerometer g Range 000: Select +/- 2g range (Default) 001: Select +/- 4g range 010: Select +/- 8g range 011: Select +/- 16g range 100: Reserved 101: Reserved 111: Reserved

Table 25. OUTCFG Resolution and Range Select Register Settings

9.11 XOFFL, XOFFH: X-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB Register	**XOFF[7]**	**XOFF[6]**	**XOFF[5]**	**XOFF[4]**	**XOFF[3]**	**XOFF[2]**	**XOFF[1]**	**XOFF[0]**	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	**XOFF[14]**	**XOFF[13]**	**XOFF[12]**	**XOFF[11]**	**XOFF[10]**	**XOFF[9]**	**XOFF[8]**	Per chip	W

9.12 YOFFL, YOFFH: Y-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB Register	**YOFF[7]**	**YOFF[6]**	**YOFF[5]**	**YOFF[4]**	**YOFF[3]**	**YOFF[2]**	**YOFF[1]**	**YOFF[0]**	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	**YOFF[14]**	**YOFF[13]**	**YOFF[12]**	**YOFF[11]**	**YOFF[10]**	**YOFF[9]**	**YOFF[8]**	Per chip	W

9.13 ZOFFL, ZOFFH: Z-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB Register	**ZOFF[7]**	**ZOFF[6]**	**ZOFF[5]**	**ZOFF[4]**	**ZOFF[3]**	**ZOFF[2]**	**ZOFF[1]**	**ZOFF[0]**	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	**ZOFF[14]**	**ZOFF[13]**	**ZOFF[12]**	**ZOFF[11]**	**ZOFF[10]**	**ZOFF[9]**	**ZOFF[8]**	Per chip	W

9.14 XGAIN: X-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB Register	**XGAIN[8]**	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	**XGAIN[7]**	**XGAIN[6]**	**XGAIN[5]**	**XGAIN[4]**	**XGAIN[3]**	**XGAIN[2]**	**XGAIN[1]**	**XGAIN[0]**	Per chip	W

9.15 YGAIN: Y-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB Register	**YGAIN[8]**	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x28	YGAIN	Y Gain Register	**YGAIN[7]**	**YGAIN[6]**	**YGAIN[5]**	**YGAIN[4]**	**YGAIN[3]**	**YGAIN[2]**	**YGAIN[1]**	**YGAIN[0]**	Per chip	W

9.16 ZGAIN: Z-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB Register	**ZGAIN[8]**	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x29	ZGAIN	Z Gain Register	**ZGAIN[7]**	**ZGAIN[6]**	**ZGAIN[5]**	**ZGAIN[4]**	**ZGAIN[3]**	**ZGAIN[2]**	**ZGAIN[1]**	**ZGAIN[0]**	Per chip	W

9.17 PCODE: Product Code

This register returns a value specific to the part number of this MEMSIC device, noted below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x3B	PCODE	Product Code Register	0	0	0	0	*	*	*	0	Per chip	R

Note: Bits denoted with '*' might be any value, set by the factory. Software should ignore these bits.

10 REVISION HISTORY

Date	Revision	Description
2014-08	APS-048-0033v1.0	First version.
2014-09	APS-048-0033v1.1	Substantial changes to magnetometer functionality.
2014-10	APS-048-0033v1.2	Added power supply pin VDDM. Changed power supply references to pins VDDM and VDDIO. Updated Typical Application Circuit with optional pullup on INTA and power supply pins. Added Order Information.
2014-10	APS-048-0033v1.3	Added ±16g range. Updated zero-g offset spec.
2015-08	APS-048-0033v1.4	Updated Tape and Reel drawings. Updated package drawing.
2016-02	APS-048-0033v1.5	Incorporated iGyro functions.
2018-07	APS-048-0033v1.6	Changed tHD;DAT (Data hold time) minimum from 5 to 0 µs
2020-03	APS-048-0033v1.7	Removed iGyro section from the datasheet
2020-08-03	APS-048-0033v1.8	Change to MEMSIC format based on the License Agreement with mCube.