2/2003

Tone Detector
Preliminary Data Sheet

MSDET

Description

The Tone Detector (MSDET) is a monolithic CMOS integrated circuit for processing analog signals before microcontroller operations. The MSDET contains an **I** and **Q** detector driven by a Voltage controlled oscillator. The center frequency of the tone detection is one-half of the VCO oscillating frequency. Center frequencies from 1 Hz to 100 kHz can be detected, and FSK decoded. The MSDET is an analog PLL with improved noise immunity when compared to a digital design.

By using the MSDET to demodulate and detect FSK or tones a slower, lower cost microcontroller can be used. This reduction in microcontroller clock rate also reduces the problems with RF emissions for FCC and CE approvals. The MSDET operates with a single supply voltage from 2.7 VDC to 5.5 VDC

The MSDET is superior to industry standard tone decoders in that control of chatter and bandwidth can be adjusted with external resistors or capacitors

The MSDET is available in a 16-pin SOIC (150 mil wide). Industrial temperature range (-40 to +85^{o}C) is available.

Features

·Low Power Consumption:
Typically less than 2.0 mW at 2.7V
·Analog PLL: Better noise immunity over simple DSP counter techniques

Applications

- Satellite radio communications
- Standard and non-standard tone detection
- Standard and non-standard FSK demodulation
- Caller ID demodulation
- Bell 103, 202 or ITU V.21, V.23 demodulation

Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature Range	-60^{o} to +150^{o} C
Operating Temperature Range	-40^{o} to +85^{o} C

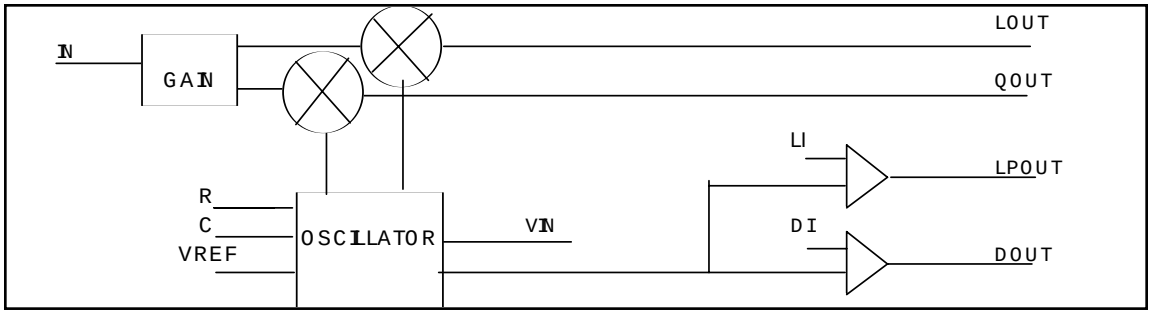

Figure 1 Block Diagram

MSDET

Electrical Characteristics

(VDD = 5.0V, T = 25^{o} C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7		5.5	V
Supply Current	IDD		0.2	0.8	2.0	mA
Digital Output Low level	VOL				0.5	VDC
Digital Output High level	VOH		0.5			VDC
Internal Voltage Reference	VREF			VDD·0.5		VDC
AC Specifications						
Input Tone Voltage			10	50	1000	mVp-p
FSK Input Impedance			10	24		kohms
VCO Minimum Frequency		R=100 kohm C=22 uF		1		Hz
VCO Maximum Frequency		R=10 kohms C= 470 pF		90		kHz
VCO Loop Gain		R=100 kohms C=1.6 nF		8		Radians/Sec/V
Phase Comparator Gain				2		V/Radians
VCO Temperature Coefficient		R=1 Mohm C=47pF		15		ppm/^{o}C

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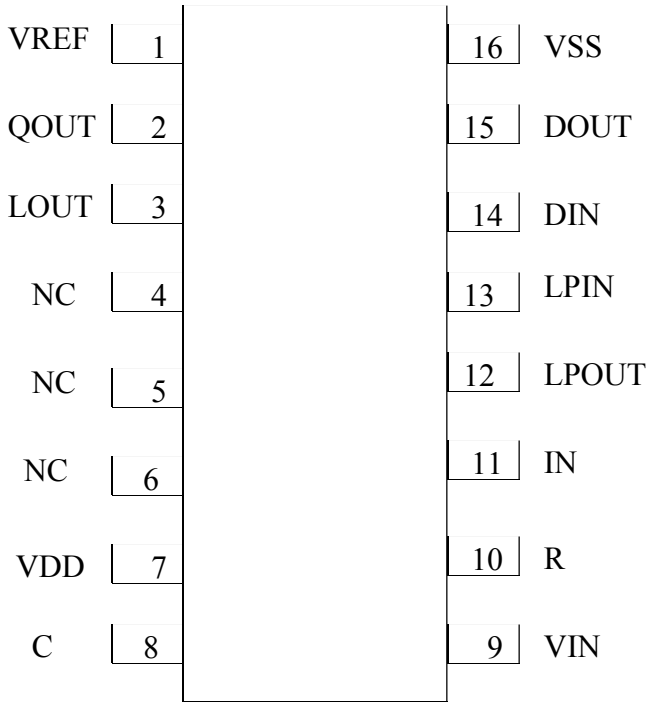
Pin Description

1	VREF	Internal Reference Voltage 1/2 VDD; Connect 1 uF to VSS from this pin.
2.	QOUT	Quadrature phase comparator Output; used for carrier lock detect.
3.	LOUT	Phase comparator Output; used to lock VCO to received signal and decode information (FM or FSK) on carrier
4,	NC	No Internal Connection
5.	NC	No Internal Connection
6.	NC	No Internal Connection
7.	VDD	Positive Power Supply. Typically 5.0 VDC
8.	C	Capacitor; for setting VCO fre-- quency, along with R (Pin 10) and VIN (Pin 9)
9	VIN	VCO Input Voltage; Filtered DC from LOUT is tied to this pin
10.	R	Resistor: For setting VCO frequency along with C (Pin 8) and VIN (Pin 9)
11.	IN	Received Signal Input: Unknown signal to be locked to the VCO for data or audio recovery
12.	LPOUT	Loop Detect Comparator Output: When output is high, coherent carrier is detected
13.	LPIN	Lock Detect Input: Filtered Quadrature Output (QOUT) is tied to this pin
14.	DIN	Data Input: Filtered Phase Comparator Output (LOUT) is tied to this pin
15.	DOUT	Data Output: Recovered FSK data
16.	VSS	Negative Supply: Typically 0 VDC

Pin Configuration



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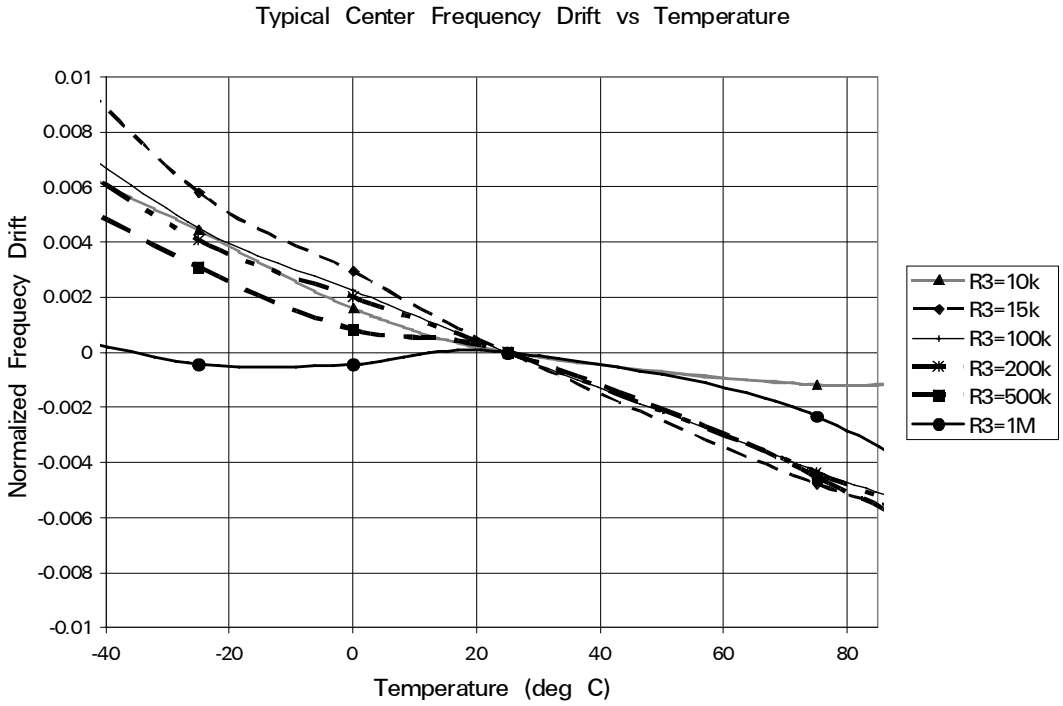

Figure 2 Graph of Temperature Coefficient with Different VCO Resistors

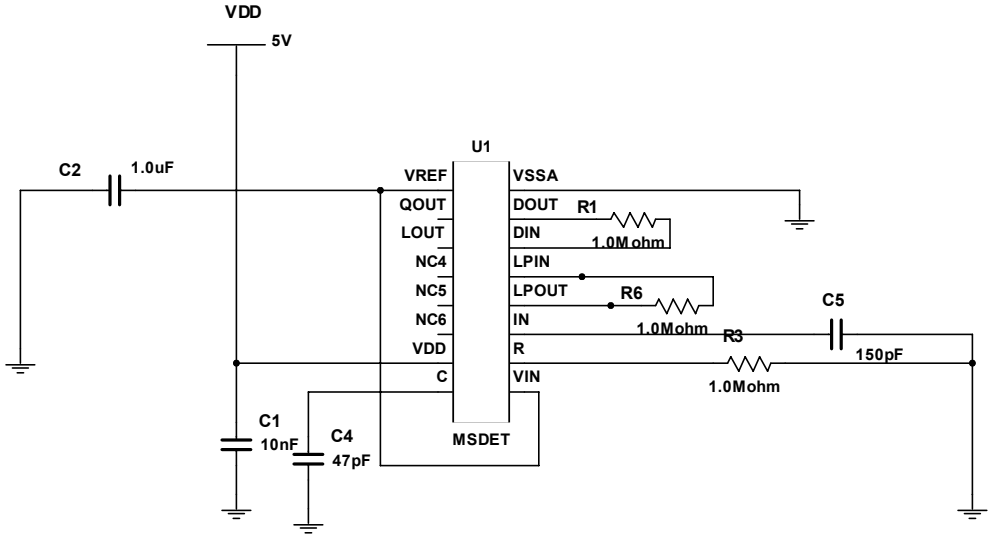

Figure 3 Schematic of circuit used for VCO Temperature Measurements

Principles of Operation

The MSDET is a phase lock loop with both Loop and Quadrature Type 2 phase detectors Type 2 phase detectors apply a limited or saturated signal to the phase comparators. This allows both FSK/FM demodulation of signals on the received carrier as well as coherent carrier detection. Coherent carrier detection is superior to Received Signal Strength Indicators (RSSI) which can provide false detection in high noise receive conditions.

Type 2 Phase detectors are sensitive to amplitude and duty cycle of the received signal. Reduced amplitude and duty cycles different than 50% will cause a reduction in the Phase detect gain, causing tracking and lock problems for the VCO. The input of the phase comparators (IN pin 11) has greater than 60 dB of gain for better sensitivity to received signals. For most FM and FSK demodulation applications, the received carrier is symmetrical (50% duty cycle). If the application of the MSDET is to lock from a clock source that is not 50%, it is best to divide the input signal by 2 and reduce the VCO frequency so lock is detected at the lower symmetrical frequency

The VCO in the MSDET oscillates at twice the detected frequency. The formula used to set the VCO frequency is:

$$f_{VCO} = 1/(3.35 \cdot R_3 \cdot C_4)$$

Component references are from Figure 4.

Flip-flops internal to the MSDET generate the quadrature clock needed for both FSK detection and coherent carrier detect. This is internally fed to two phase comparators. The center frequency of the tone detection is half the VCO oscillating frequency. The LOUT of the MSDET is filtered and tied to VIN to close the loop and allow the phase error to control the VCO frequency.

With all analog PLL there is a tendency to lock to third-harmonic of the desired tone. By using external filters and coupling capacitors, this characteristic can be minimized. Figure 4 is a typical schematic for the MSDET in FSK mode. A low-value input coupling capacitor is used to apply received signals to the input gain stage. This reduces VCO sub-harmonic lock, where the VCO is locked at 1/3 the frequency of the third harmonic.

Unlike other PLLs on the market, the MSDET has a true Voltage controlled oscillator, not a Current Controlled oscillator (CCL). A VCO allows a larger range of resistors for tracking adjustment.

Selection of Filter Components

The MSDET provides maximum flexibility in setting the VCO frequency, speed of carrier lock detect, Loop damping, tracking range, capture range, and reduction in possible chatter on the Data and Lock outputs. Unlike other PLLs the output comparators, lock detect and VCO are completely isolated The MSDET permits the adjustment of the external resistor and capacitors at QOUT, LOUT and VIN.

The outputs QOUT and LOUT are at CMOS levels. QOUT is the exclusive-or of the input and the Quadrature phase of the VCO frequency (divided by 2). LOUT is the exclusive-or of the input and the VCO frequency (divided by 2). The outputs are filtered and compared with VREF voltage, in order to detect carrier and determine if a logic 0 or 1 frequency is received (LOUT) or a coherent carrier is detected (QOUT).

For optimum performance under high noise conditions, the loop bandwidth should be as narrow as possible. However, for preventing FSK errors due to tracking, the loop should be as wide as possible. SInce it is not possible to achieve both with the same components, a compromise must be made. If the application is a tone detector, then making the tracking bandwidth narrow will improve signal-to-noise performance.

If the received signal is frequency shift keying (FSK), then the bandwidth must be adjusted wider to allow tracking of the two tones as well as possible frequency error of the transmitter, carrier offset caused by changes in media (eg: copper to radio wave) and mis-setting of the MSDET VCO.

As Figure 4 is studied, more than one filter can be seen connected to LOUT. The tracking filter is achieved with R1 and C6 (Figure 4 references). The filter for reducing data chatter is controlled by R2 and C3. The data filter is set at a much lower frequency than the data rate, since the comparator can detect small changes in voltage.

The lock detect filter is separate from the tracking filter. Typically one delays the Lock Detect output in order to prevent capturing data that is incorrect. This delay is controlled by R10, R11 and C7 (Figure 4).

FSK Example Calculation:

For a radio link with a frequency bandwidth of less than 50 kHz, the maximum data rate using the MSDET in FSK mode is 50 kbps.

In order to have enough cycles of the carrier frequency for detection select a Mark (logic high or 1) frequency of 78 kHz and a space (Logic low or 0) frequency of 50 kHz. The VCO is set for 64 kHz (center frequency between the mark (logic high or 1) and space (logic low or 0) frequency). Using the formula:

$$f_{VCO} = 1/(3.35 \cdot R_3 \cdot C_4)$$

And referencing the effect of R3 value to TCO (Figure 2)

$$64kHz = 1/(3.35 \cdot 100k \cdot C_4)$$

$$C_4 = 47\ pF$$

Since there is no additional encoding (1 bit/baud or symbol) the bandwidth needed for data is 50 kHz. But, with the higher input gain of the MSDET, placing the corner frequency at 5kHz provides better performance than setting the low-pass filter corner frequency equal to the data rate. Using the first order filter formula:

$$fc = 1/(2 \cdot \pi \cdot R1 \cdot C6)$$

The voltage to the VCO is adjusted with R8 and R4. The VCO conversion gain allows for the VCO to lock to frequencies from 32 to 96 kHz This could cause data errors by locking to noise on the line. Since only 28 kHz is needed for tracking, the phase detector tracking range is reduced to 50kHz.

$$f_{TRACK} = \Delta f_{VCO} \cdot R4/(R4+R8)$$

This allows tracking of the 28 kHz frequency change of the data rate as well as the initial capture of the incoming signal.

The data filter is set to attenuate the carrier as much as possible (as well as the error voltage which contains the data information) in order to eliminate chatter.

$$f_{DATA} = 1/(2 \cdot \pi \cdot R2 \cdot C3)$$

$$f_{DATA} = 2kHz$$

By setting the corner at approximately 1/10 the equivalent data rate (50 kbps "U" (ASCII Hex 0x55) pattern is a 25 kHz square wave), chatter on the comparator output is eliminated but the data is recovered.

Lock Detect should be set to delay output until enough cycles are received to be detected.

$$t = R10 \cdot C7$$

The amount of delay is dependent upon the data received. If the data has 50 ms preamble of ASCII character "U" (hexadecimal 0x55), then the lock detect time delay can be up to 50 ms. If data starts immediately, then the shortest time is set, and data is qualified by a microprocessor.

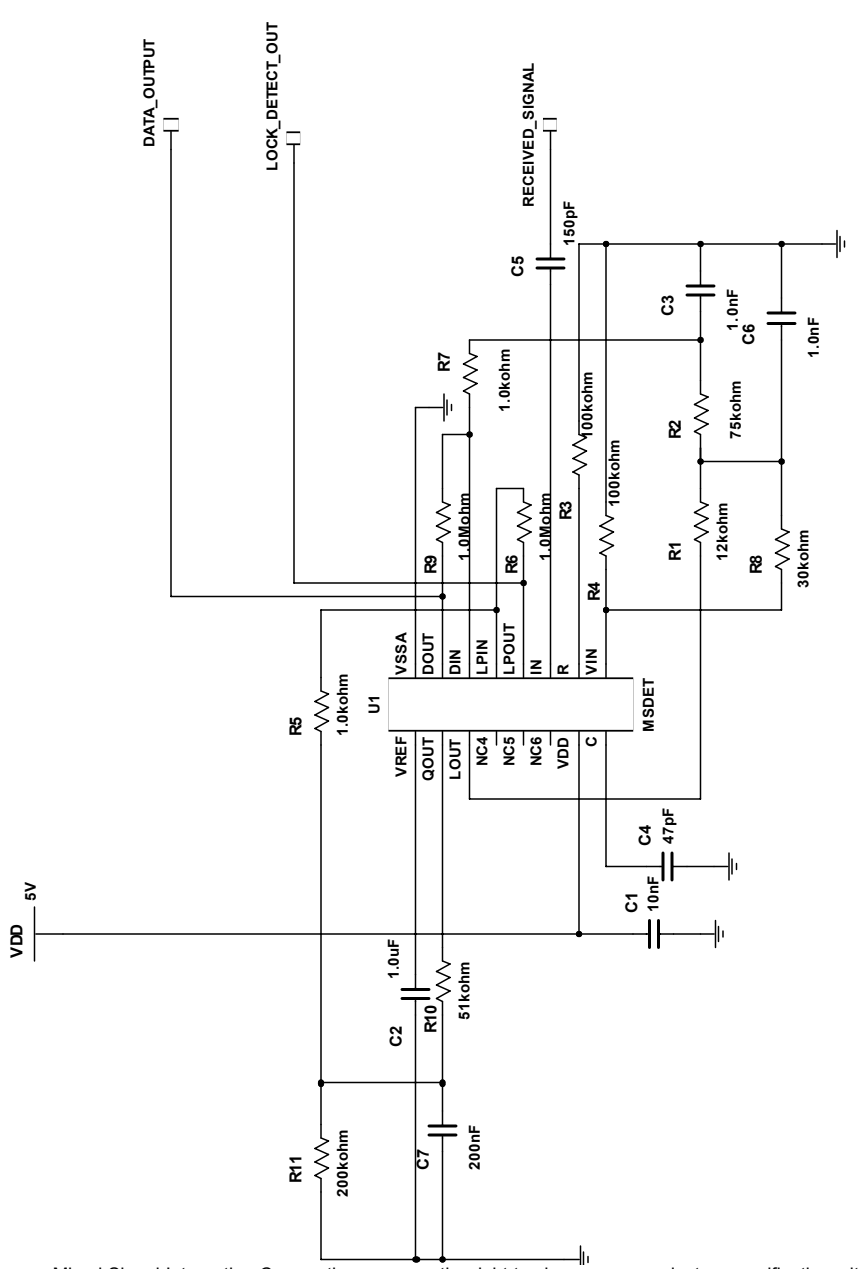

Figure 4 Typical Application Schematic for FSK Demodulation and Carrier Lock Detection

MSDET

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MSDET

STANDARD PRODUCTS	
MSGEQ5A	Five Band Graphic Equalizer
MSGEQ7	Seven Band Graphic Equalizer
MSHFS1-6	Selectable High Frequency LP/BP Filter
MSFS1-6	Selectable Lowpass/Bandpass Filter
MSCAHF	Selectable High Frequency Active Lowpass/Bandpass Filter
MSU1F1-4, MSU2F1	Resistor Programmable Universal Active Filter
MSU1HF1-4, MSU2HF1	High Frequency Resistor Programmable Universal Active Filter
MSELP	Switched Capacitor Elliptic Lowpass Filter with Op Amps
MSNBLP	Switched Capacitor Butterworth Lowpass Filter
MSLE/B/C5L/M	Switched Capacitor General Purpose Lowpass Filter
MS2LFS	Dual Selectable Low Voltage Lowpass/Bandpass Filter
MSHN1-6	Selectable High Pass/Notch Filter
MSRAAF	Resistor Programmable Active Audio Filter
MSRAHF	Resistor Programmable Active High Frequency Filter
MSDET	Tone Decoder
MS2CAP	Two Channel Audio Processor

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