Dual Selectable Low Voltage Lowpass/Bandpass Filter
Data Sheet

MS2LFS

Description

The dual selectable lowpass/bandpass filter IC is a CMOS chip that can be configured for either a lowpass or a bandpass filter. Each filter is selectable independently. The lowpass response can be a 7 pole Butterworth, Elliptic or Bessel filter. The band pass response can be a six pole full, third or sixth octave bandpass filter. The device uses switched-capacitor filters and no external components (except for decoupling capacitors) are required, Only an external CMOS level clock is needed.

An externally selectable gain setting pin, a power down pin and clock to corner ratio select pin are included. Typical current consumption is as low as 500 uA and the minimum operating voltage is 1.1 volts, making the device ideal for portable applications.

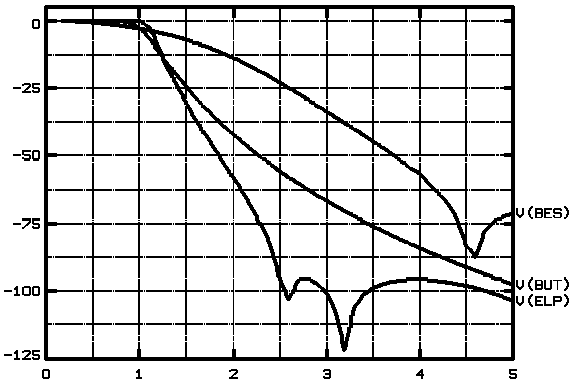
Features

Two Independent Filters
Six Filter Types In One Package
No External Components
Switched-Capacitor Filters
Low Power Operation
Low Voltage Operation
Adjustable Gain 0, 6 or 12 dB
Small Package Size
Low Cost
On Chip Power Save Pin
ANSI Compatible Bandpass
Op Amp Input

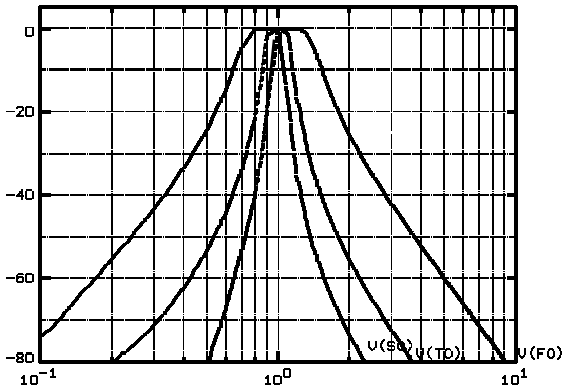
Applications

Spectrum Analyzers
Battery powered General Purpose Systems
Portable Systems
Anti-Alias Filters
Reconstruction Filters
Telecommunications (Cell phone ASP)
Tracking Filters
Harmonic Analysis
Noise Analysis
Data Communication
Wireless Applications
Telemetry

Lowpass Responses



Bandpass Responses



Electrical Characteristics

(VDD = +1.2V, T = 25° C)

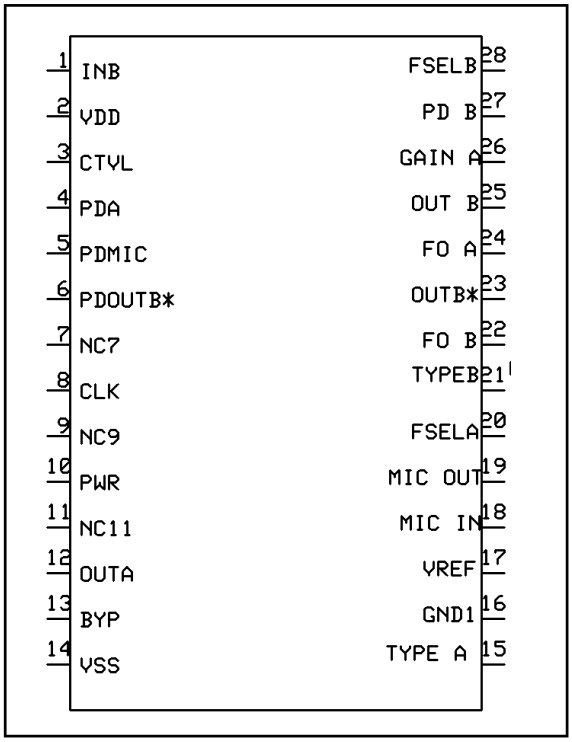
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		1.1	1.2	3.6	V
Supply Current	IDD	VDD = 3.3V, CTVL = 0, PWR = 1		2.7		mA
Supply Current	IDD	VDD = 1.1V, CTVL = 1, PWR = 1		1100		uA
Supply Current Low Power Mode	IDD	VDD = 3.3V, CTVL = 0, PWR = 0		1		mA
Supply Current Low Power Mode	IDD	VDD = 1.1V, CTVL = 1, PWR = 0		200		uA
Supply Current Power Down Mode	IDD	PDA=PDB=0, CTVL=0		50		uA
AC Specifications						
Gain	Av		-0.5	0	0.5	dB
Noise		To 1/2 Sample		200		uVrms
Distortion	THD			-62		dB
Signal Swing		1 kHz, VDD = 1.2V	800			mV p-p
Input Impedance	ZIN			1		Mohm
Output Drive	Io			1		mA
Output Impedance	Zo			500		ohm
Output Capacitive Load				22		pF
Clock to Corner *		Fo=1		85.3		Hz/Hz
Clock to Corner *		Fo=0		42.65		Hz/Hz
Center Frequency Range	Fo		0.001		6	kHz
Ripple						
Elliptic Lowpass				0.2		dB
Full Octave				0.2		dB
Third Octave				0.2		dB
Sixth Octave				0.2		dB
Stop Band Rejection						
Elliptic/Butterworth Lowpass		fCLOCK = 2.048 MHz		75		dB
Bessel Lowpass		fCLOCK = 2.048 MHz		65		dB
40 dB Bandwidth						
Full Octave		Normalized Fo	0.3		3	
Third Octave		Normalized Fo	0.6		1.67	
Sixth Octave		Normalized Fo	0.76		1.32	
Bandpass Q						
Full Octave Q	Q			1.5		
Third Octave	Q			4.5		
Sixth Octave	Q			9		

* External clock is 8X internal clock

Pin Description

1. IN B	Filter Input B
2. VDD	Positive Power Supply, typically 1.2 Volts for Single Supply
3. CTVL	Activate or Disable Boost Circuit Disable = 0, Activate = 1
4. PDA	Power Down Filter A
5. PD MIC	Power Down Mic Amp
6. PD $\overline{\text{OUTB}}$	Power Down $\overline{\text{Output B}}$
7. NC	
8. CLK	Clock Input
9. NC	
10.PWR	Sets Bias Current for Filter Stages Lo=low power, Hi=normal power
11. NC	
12. OUT A	Filter Output A
13. BYP	Bypass Capacitor for Boost Circuit, voltage at this pin is negative in relation to VSS, tie positive side of polarized cap to VSS
14. VSS	Ground Pin, 0 Volts for Single Supply
15. TYPE A	Filter Response Select Pin for Filter A
16. GND1	AC Ground, decouple with 0.1 uF to VSS
17. VREF	Reference Voltage, internally generated, typically VDD/2.2 for Single Supply Operation, decouple with 0.1 uF to VSS
18. MIC IN	Input of MIC Amp
19. MIC OUT	Output to MIC Amp
20. FSEL A	Selects Filter. 0 = Low Pass, 1 = Band Pass
21. TYPE B	Filter Response Select Pin for Filter B
22. FO B	Clock to Corner Select Pin for Filter B
23. $\overline{\text{OUT B}}$	Filter B Output 180 degrees out of phase from OUT B
24. FO A	Clock to Corner Select Pin for Filter A
25. OUT B	Filter B Output
26. GAIN A	Filter A, Gain Select Pin
27. PD B	Power Down, Filter B
28. FSEL B	Selects Filter 0 = Low Pass, 1 = Band Pass

Pin Configuration



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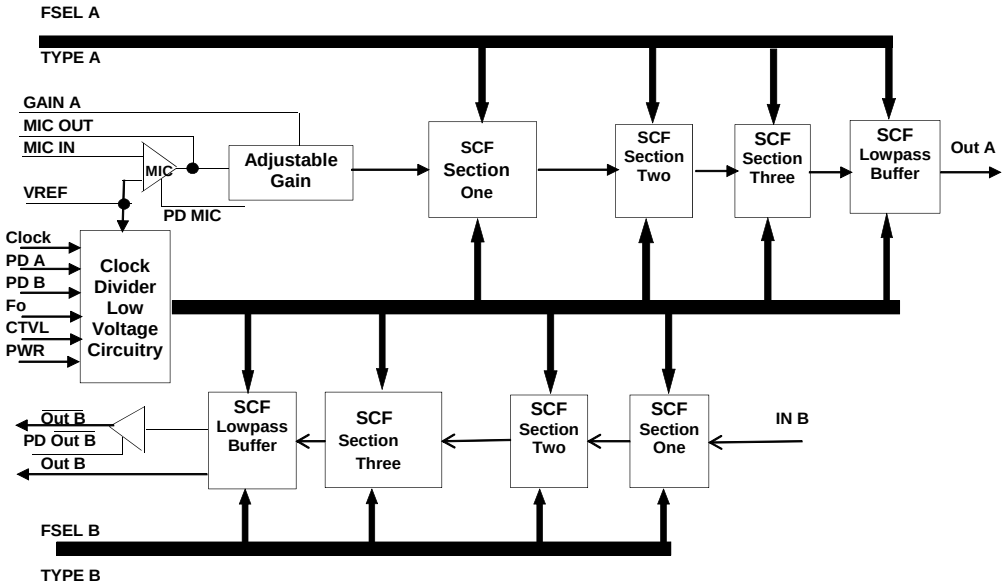
Block Diagram



Absolute Maximum Ratings

Power Supply Voltage	+5V
Storage Temperature	-60 to +150 C
Operating Temperature	0 to 70C

Ordering Information

Part Number	Package
MS2LFSP	28 Pin DIP
MS2LFSS	28 Pin 300 mils wide SOIC

Filter Selection

The filter type is selected using the two filter select pins, TYPE and FSEL, FSEL is a CMOS level pin that selects lowpass or bandpass (lowpass = 0, bandpass = 1). TYPE Is a tertiary control pin that selects the filter response. State 0 is VSS, state 1 is GND and state 2 is VDD.

	FSEL=0	FSEL=1
TYPE	Lowpass	Bandpass
0	Butterworth	Full Octave
1	Bessel	Third Octave
2	Elliptic	Sixth Octave

Digital Levels

All the clock and control pins are referenced between VSS and VDD. In single supply applications, the digital levels should be CMOS levels from VSS to VDD. The tertiary controls (pins - TYPE and GAIN) should be set at VSS, VREF or VDD depending on the filter type or gain de-

Gain and Frequency Selection

The Gain control pin G is a tertiary control pin where state 0 is VSS, state 1 is GND level and state 2 is VDD.

G	Gain
0	OdB
1	6dB
2	12dB

The frequency control pin F0 is a CMOS level pin where high is clock to corner of 85.3 to 1 (170.6 to 1 for Bessel) and low is clock to corner of 42.65 to 1 (85.3 to 1 for Bessel).

Application Schematic