

Switched Capacitor General Purpose Lowpass Filter

Advance Data Sheet

Description

The general purpose lowpass filter is a 5 pole filter made in CMOS technology. It uses a switched capacitor filter implementation. No external components are necessary to set the filter characteristics. The cutoff frequency of the lowpass filter is selectable based on the clock frequency. The clock to cutoff frequency ratio can be selected at either 50:1 or 100:1 by using the Clock to Corner Select pin. Either an external clock or the on-chip oscillator can be used. Three popular filter responses are available - elliptic (E), Butterworth (B) and Chebyshev (C). Low frequency versions (L) have a maximum corner frequency of 5 kHz. Medium frequency versions (M) have a maximum corner frequency of 20 kHz. Parts are packaged in either DIP or SOIC.

Features

- No response setting resistors
- Plastic DIP or S.O. packages available
- Switched Capacitor Filters
- 3.3 or 5 Volts Operation
- Operates from internal or external clock
- Elliptic, Butterworth or Chebyshev responses

Applications

- Instrumentation
- Telecommunications
- Anti-Alias Filters
- General Purpose Low-Pass Filters

Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature	-60 to +150°C
Operating Temperature	0 to 70°C

Ordering Information

Part Number	Type	Package	Operating Temperatures
MSLE5LP	Elliptic	8 Pin DIP	0 to 70°C
MSLE5LS	Elliptic	8 PIN SOIC	0 to 70°C
MSLE5MP	Elliptic	8 PIN DIP	0 to 70°C
MSLE5MS	Elliptic	8 PIN SOIC	0 to 70°C
MSLB5LP	Butterworth	8 PIN DIP	0 to 70°C
MSLB5LS	Butterworth	8 PIN SOIC	0 to 70°C
MSLB5MP	Butterworth	8 PIN DIP	0 to 70°C
MSLB5MS	Butterworth	8 PIN SOIC	0 to 70°C
MSLC5LP	Chebyshev	8 PIN DIP	0 to 70°C
MSLC5LS	Chebyshev	8 PIN SOIC	0 to 70°C
MSLC5MP	Chebyshev	8 PIN DIP	0 to 70°C
MSLC5MS	Chebyshev	8 PIN SOIC	0 to 70°C

MSLE5L/M,MSLB5L/M,MSLC5L/M



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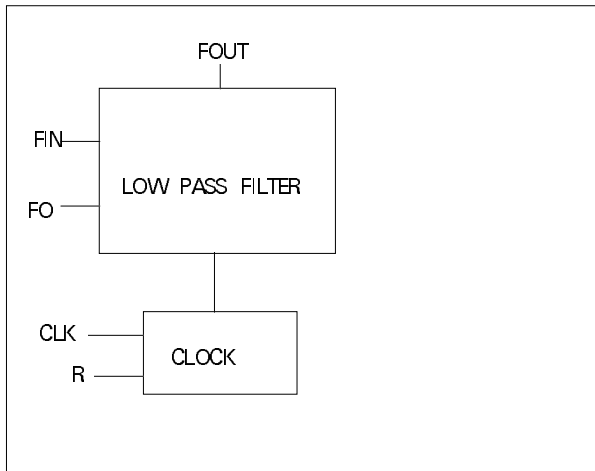
MSLE5L/M,MSLB5L/M,MSLC5L/M

Electrical Characteristics

(VDD = +5.0V, T = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7		5.5	V
Supply Current	IDD	L versions	100	300	1000	uA
		M versions	0.5	1.0	2.0	mA
AC Specifications						
Gain	Av		-1	0	1	dB
Maximum Corner Frequency	fo max	L versions	3	5		kHz
		M versions	10	20		kHz
Clock Feedthrough - Filter Output		Pedestal to Pedestal		10		mV (p-p)
Clock to Corner	fCLK/fo	FO = LOW	99	100	101	Hz/Hz
		FO = HIGH	49	50	51	Hz/Hz
Offset Voltage			-10		10	mV
Output Voltage Swing			4.0	4.5		Vp-p
Level Shift Threshold	VTL-to-VTH		1.6	2.0	2.4	V
	VTH-to-VTL		2.2	3.0	3.7	V
	VTL-to-VTH	VDD = 2.7V	0.6	1.0	1.25	V
	VTH-to-VTL	VDD = 2.7V	1.4	1.75	2.08	V

Block Diagram

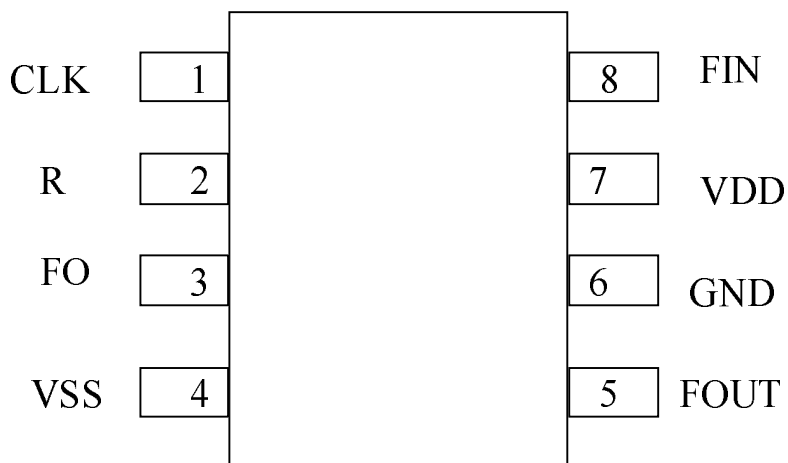


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Pin Description

1	CLK	Clock Input
2	R	Connection for the Clock Resistor (NC when using external clock)
3	FO	Clock to Corner Select Pin, CMOS level (NC is FO = HIGH)
4	VSS	Negative Power Supply, Typically -2.5V for Split Supplies, 0V for Single Supply
5	FOUT	Filter Output
6	GND	Ground Pin 0V for Split Supplies Typically 2.5V for Single Supply
7	VDD	Positive Power Supply, Typically 2.5V for Split Supplies, 5V for Single Supply
8	FIN	Filter Input

Pin Configuration

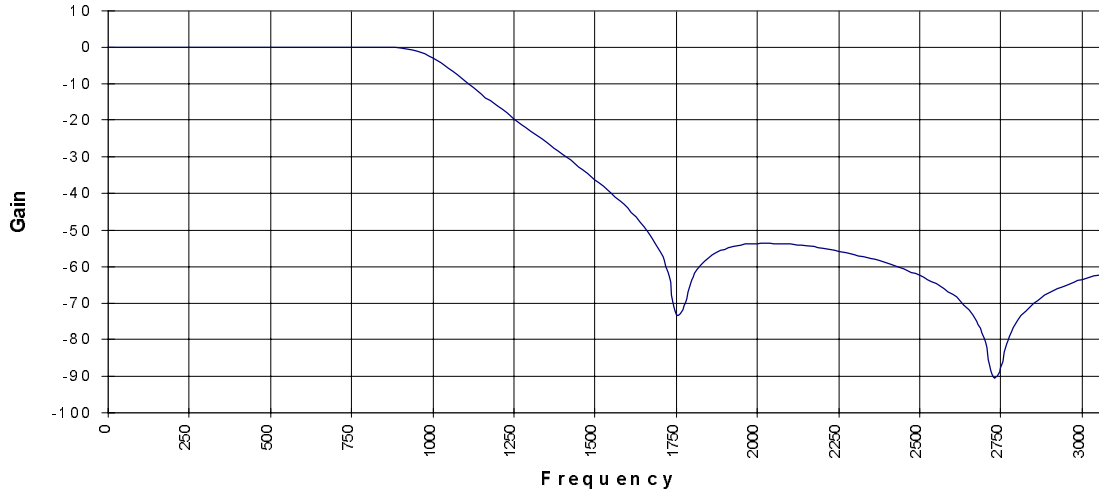

MSLE5L/M,MSLB5L/M,MSLC5L/M



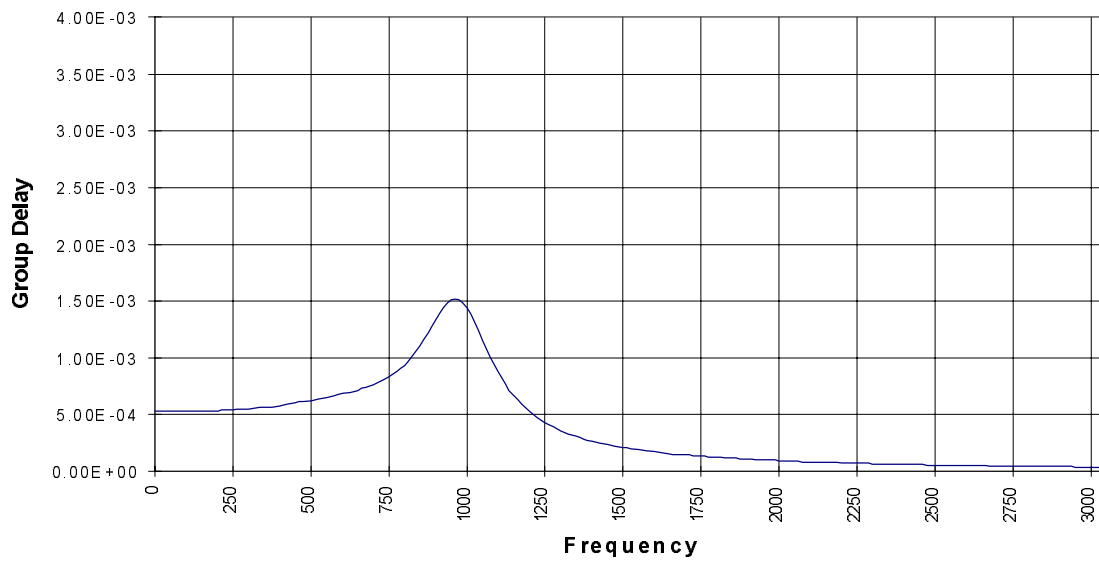
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MSLE5L/MSLE5M Frequency Response



MSLE5L/MSLE5M Group Delay

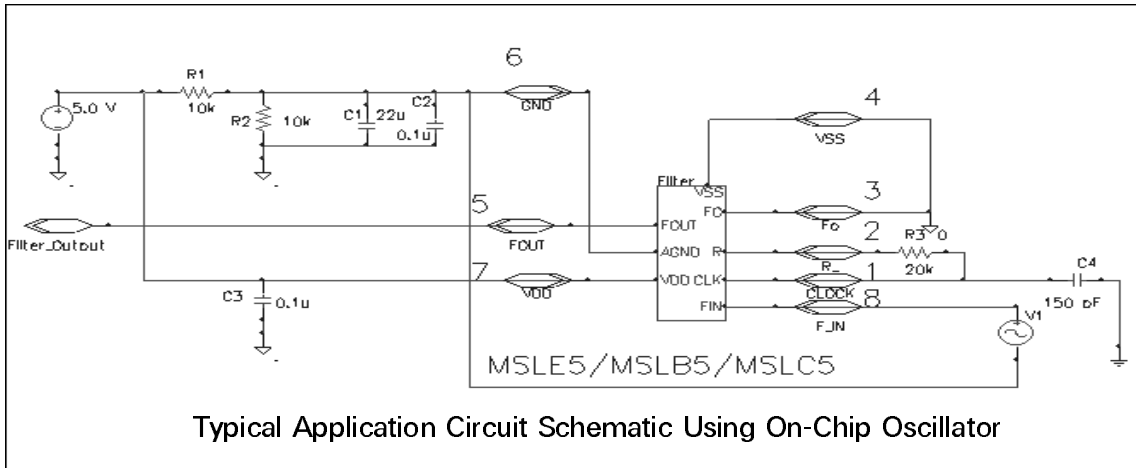


MSLE5L/M,MSLB5L/M,MSLC5L/M

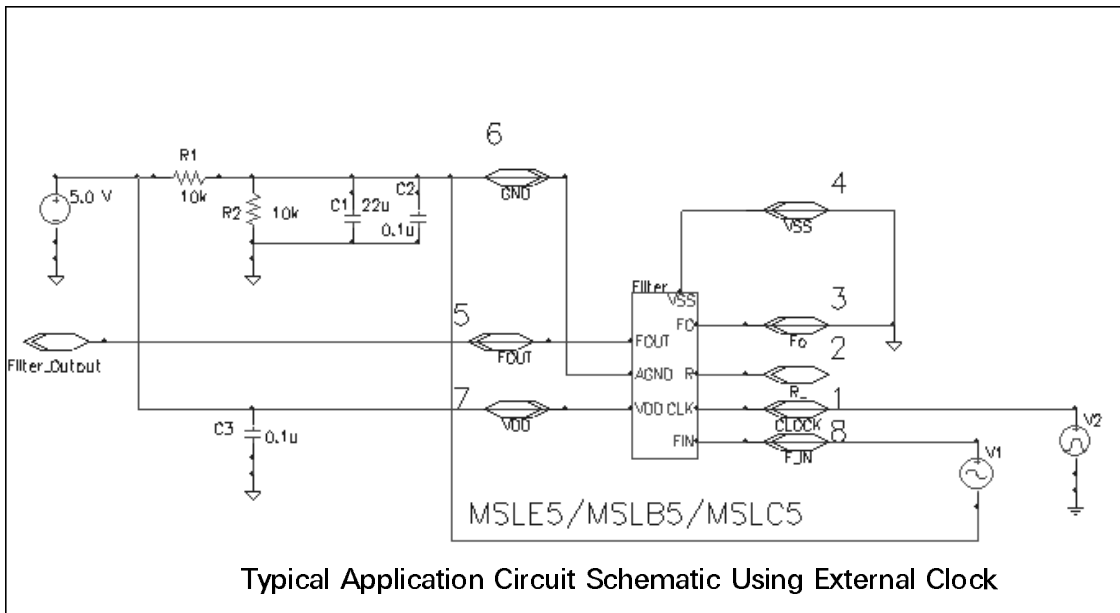


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MSLE5L/M, MSLB5L/M, MSLC5L/M



Typical Application Circuit Schematic Using On-Chip Oscillator



Typical Application Circuit Schematic Using External Clock