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Switched Capacitor Butterworth Lowpass Filter
Data Sheet

MSNBLP

Description

The lowpass filter has a non-inverting butterworth response and is made in CMOS technology. It uses a switched capacitor filter implementation. No external components are necessary to set the filter characteristics. The cutoff frequency of the lowpass filter is selectable based on the clock frequency. Either an external clock or the on-chip oscillator can be used. Included in the integrated circuit are two op amps which can be configured by the user.

The clock to cutoff frequency ratio can be selected at either 50:1 or 100:1 by using the Clock to Corner Select pin. A current-saving power down mode can be chosen with the Power Select pin. In the low power mode the maximum corner frequency is 5 kHz. In regular operation the maximum corner frequency is 20 kHz.

Features

No response setting resistors needed
Switched Capacitor Filters
3.3 or 5 Volts Operation
Operates from internal or external clock
Includes two uncommitted op amps
Power down mode
Selectable clock to corner frequency ratio

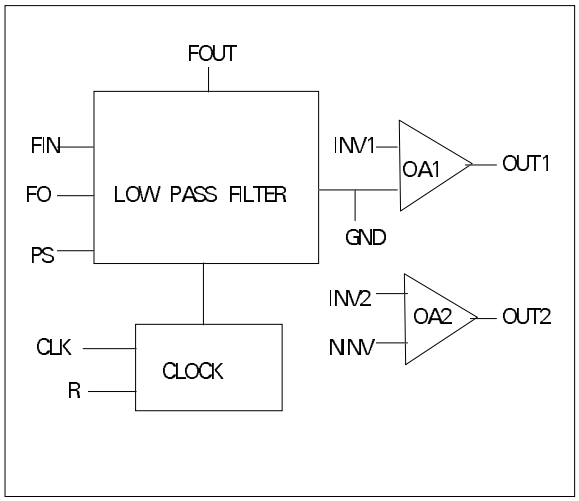
Applications

Two Way Radio
Telecommunications
Data Communications
Anti-Alias Filters
General Purpose Low-Pass Filters

Absolute Maximum Ratings

Power Supply Voltage	+6 V
Storage Temperature	-60 to +150°C
Operating Temperature	-40 to +85°C

Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
MSNBLPS	14 Pin 300 mil SOIC	-20 to +75°C

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Electrical Characteristics

(VDD = +5.0V, T = 20 °C)

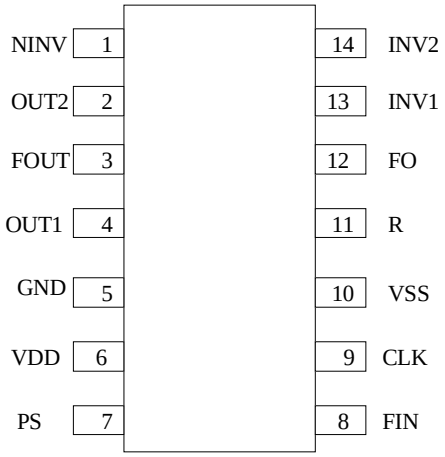
PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7		5.5	V
Supply Current	IDD	PS = 0.5 State	0.2	0.6	1.0	mA
		PS = 1 State	0.8	1.0	2.0	mA
		PS = 0 State	100	250	400	uA
AC Specifications						
Gain	Av	Fclk = 250 kHz	-0.75	0	0.75	dB
Maximum Corner Frequency	fo max	PS = 0.5 State	3	5		kHz
		PS = 1 State FO=HIGH	10	20		
Clock Feedthrough		Pedestal to Pedestal				
- Filter Output		Fclk = 1 MHz		10		mV (p-p)
- Op Amp 1 Output				10		mV (p-p)
- Op Amp 2 Output				10		mV (p-p)
Clock to Corner	fCLK/fo	External Clock, FO = LOW	99	100	101	Hz/Hz
		External Clock, FO = HIGH	49	50	51	Hz/Hz
Offset Voltage				90	150	mV
Output Voltage Swing		PS = 1 State, FO = LOW	3.5	4.0		V p-p
Dynamic Range				82		dB
Op Amp Specifications						
Input Offset Voltage	Vos			10		mV
Output Voltage Swing				4.5		Vp-p
Slew Rate				6		V/uS
DC Gain				70		dB
Gain Bandwidth	bw			1.2		MHz
Level Shift Threshold						
	VTL-to-VTH		1.1	1.3	1.7	V
	VTH-to-VTL		3.3	3.8	4.3	V
	VTL-to-VTH	VDD = 2.7V	0.75	0.85	0.95	V
	VTH-to-VTL	VDD = 2.7V	1.5	1.8	2.1	V
Power Select Pin Operation						
State 1 High Power	PS	Voltage on PS Pin		VDD		V
State 0.5 Low Power				GND		V
State 0 Power Down		See note		VSS		V

Note: In external clock mode only. Power down is not available in on chip oscillator mode.

Pin Description

1	NINV	Second Op Amp Non Inverting Input
2	OUT2	Second Op Amp Output
3	FOUT	Filter Output
4	OUT1	First Op Amp Output
5	GND	Ground Pin, 0V for Split Supplies Typically 2.5V for Single Supply
6	VDD	Positive Power Supply, Typically 2.5V for Split Supplies, 5V for Single Supply
7	PS	Power Select Pin (See Electrical Characteristics)
8	FIN	Filter Input
9	CLK	Clock Input
10	VSS	Negative Power Supply, Typically -2.5V for Split Supplies, 0V for Single Supply
11	R	Connection for the Clock Resistor (NC when using external clock)
12	FO	Clock to Corner Select Pin, CMOS level
13	INV1	First Op Amp Inverting Input
14	INV2	Second Op Amp Inverting Input

Pin Configuration



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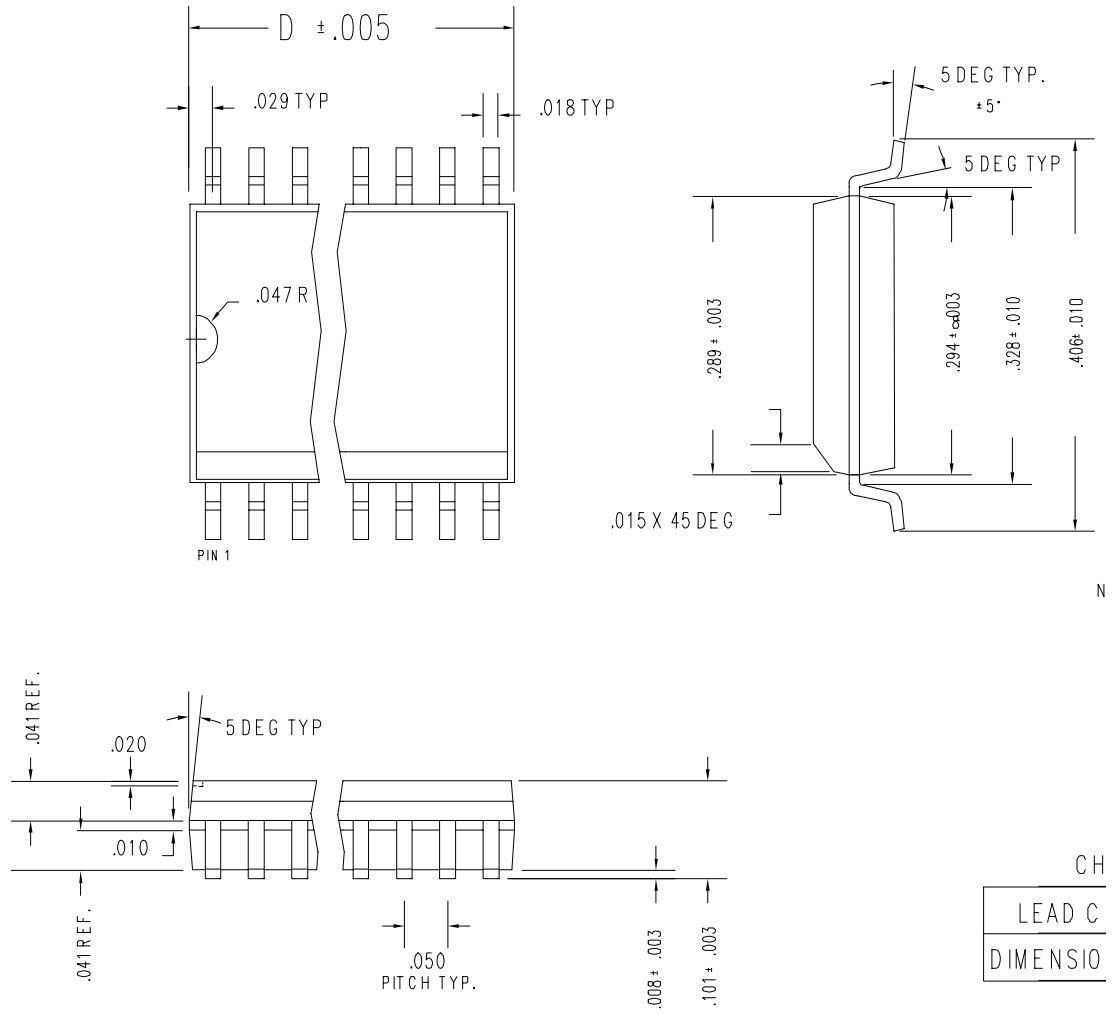

External Package Dimensions for 14 lead, 300 mils wide, "S" plastic SOIC package. Dimension D = .354, all dimensions in inches.