Resistor Programmable Active Audio Filter
Preliminary Data Sheet

MSRAAF

Description

The resistor programmable continuous audio active filter IC Is a CMOS chip that can be configured for either a lowpass, bandpass, highpass, allpass or notch filter. Butterworth, Bessel, elliptic and Chebyshev filters can be implemented. The frequency range covers the audio spectrum to 20 kHz. There is a low power version with a frequency range to 5 kHz. There is a power down pin to reduce current consumption when the filter is not in use. The 8 pin part is a single filter stage, the 16 pin part offers a dual filter stage. Between 2 and 5 external resistors set the filter characteristics depending on the desired response. Q can be set from between 0.25 and 50. No clock signal is required.

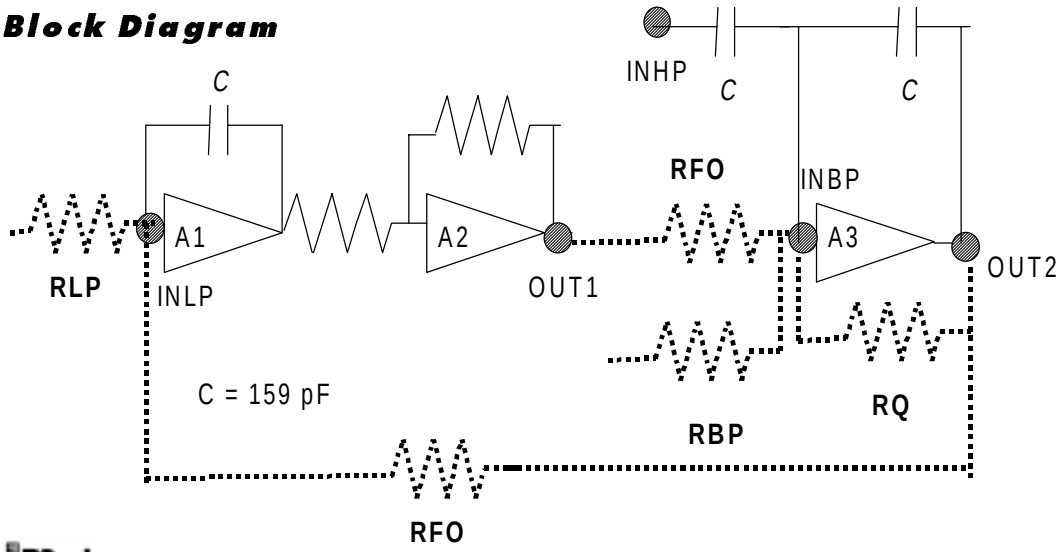
Features

Independent Q, frequency and gain adjustments
Low sensitivity to external resistor variation
Operates up to 20 kHz
Q range from 0.25 to 50
Low Power Operation
Low Voltage Operation
On Chip Power Save Pin
Cascadable for Higher Order Filtering

Applications

Spectrum Analyzers
General Purpose Systems
Portable Systems
Anti-Alias Filters
Reconstruction Filters
Telecommunications
Tracking Filters
Harmonic Analysis
Noise Analysis
Data Communication
Wireless Applications

Block Diagram



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Electrical Characteristics

(VDD = +5.0V, T = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7	5	5.5	V
Supply Current	IDD	MSRAAF1; or MSRAAF2 and PWR = HI		2		mA
Supply Current	IDD	MSRAAF3, or MSRAAF2 and PWR = LO		220		uA
Power Down Current		PD = HI		100		uA
AC Specifications						
Gain	Av		-0.5	0	0.5	dB
Signal to Noise Ratio				95		dB
Distortion	THD				0.1	%
Signal Swing		1 kHz	3.5	4		V p-p
Input Impedance	ZIN	fIN = 1 kHz		1		Mohm
Output Drive	Io			1		mA
Output Impedance	Zo	fIN = 1 kHz		500		ohm
Output Capacitive Load				50		pF
Center Frequency Range	Fo	PWR = HI	50		80	kHz
Center Frequency Range	Fo	PWR = LOW	50		10	kHz
fo Accuracy				+/- 3		%
Q Range	Q		0.25		50	

msi

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Pin Description

16 Pin Package

1.	VDDA	Positive Power Supply, Typically 2.5 Volts for Split Supply, 5.0 Volts for Single Supply
2.	OUTA 2	Output 2 for Channel A
3.	OUTA 1	Output 1 for Channel A
4.	INBPA	Bandpass Input for Channel A
5.	INHPA	Highpass Input for Channel A
6.	INLPA	Lowpass Input for Channel A
7.	VSS	Negative Power Supply, Typically -2.5 Volts for Split Supply. 0 Volts for Single Supply
8.	PD	Power Down Pin, CMOS level, Hi = Power Down
9.	GND	GND Pin, OV for Split Supplies 2.5 Volts Typical for Single Supply
10.	BIAS	Bias Pin (OPEN)
11.	INLPB	Low Pass Input for Channel B
12.	INHPB	High Pass Input for Channel B
13.	INBPB	Band Pass Input for Channel B
14.	OUTB 1	Output 1 for Channel B
15.	OUTB 2	Output 2 for Channel B
16.	PWR	Set Bias Current for Filter Stages, LO=Low power, HI=normal power

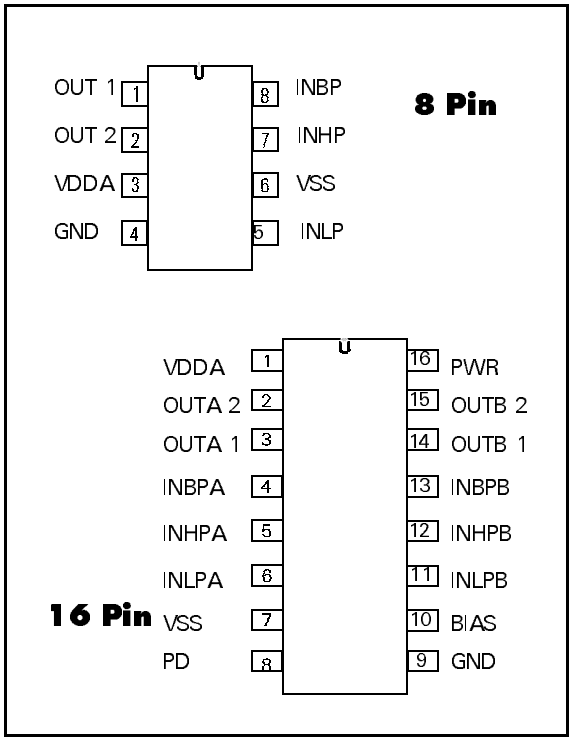
8 Pin Package

1.	OUT 1	Output 1
2.	OUT 2	Output 2
3.	VDD	Positive Power Supply, Typically 2.5 Volts for Split Supply, 5.0 Volts for Sin gle Supply
4.	GND	Ground Pin, 0V for Split Supplies, 2.5 Volts Typical for Single Supply
5.	INLP	Low Pass Input
6.	VSS	Negative Power Supply, Typically -2.5 Volts for Split Supply, 0 Volts fc ingle Supply
7.	INHP	High Pass Input
8.	INBP	Band Pass Input

Ordering Information

Part Number	Package
MSRAAF1P	8 Pin DIP
MSRAAF2P	16 Pin DIP
MSRAAF3P	8 Pin DIP
MSRAAF1S	8 Pin SOIC
MSRAAF2S	16 Pin SOIC
MSRAAF3S	8 Pin SOIC

Pin Configuration



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RFO = 1E9/Fo RA = RFO

RQ = Q * RFO

LOWPASS KLP = Lowpass Gain

RLP = RFO/KLP ; RBP = ∞ ; INHP to GND

BANDPASS KBP = Bandpass Gain

RBP = RFO/KBP * Q ; RLP = ∞ ; INHP to GND

HIGH PASS Gain = 1

RLP = ∞ ; RBP = ∞

NOTCH

RLP = RFO ; RBP = ∞

ALL PASS

An External Op Amp Inverter is required

RLP = RFO ; RBP = RQ ; R1 = R2

LOW PASS NOTCH

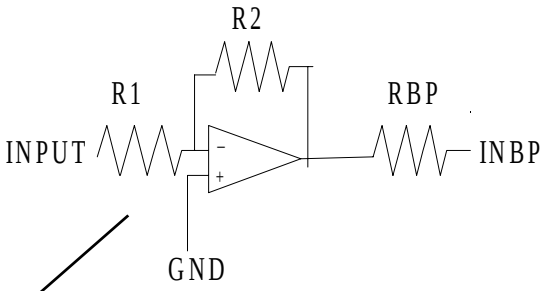
An External Resistor Divider is required on INHP

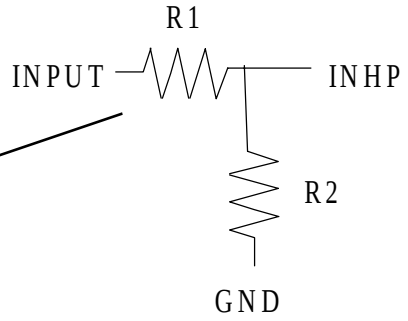
RLP = RFO ; RBP = ∞

FZ = Fo * (R2/(R1 + R2))**1/2 ;

HIGHPASS NOTCH

RLP = {(Fz/Fo)** (1/2)} * RFO ; RBP = ∞





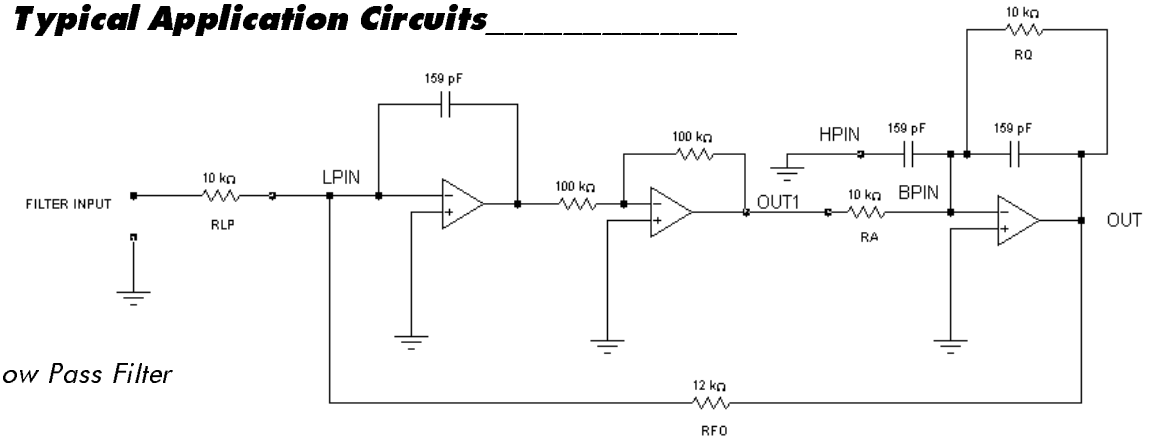
Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature	-60 to +150 C
Operating Temperature	0 to 70 C

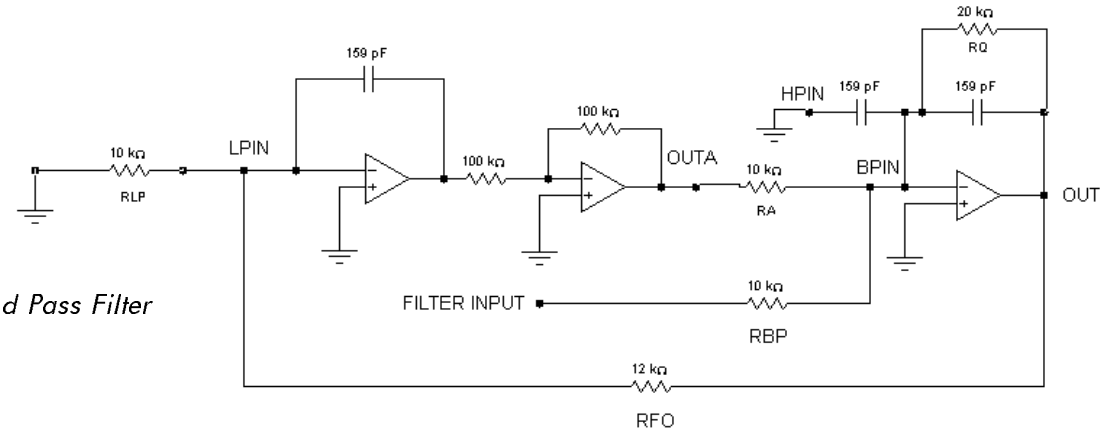
Digital Levels

The PD is referenced between GND and VDD. In single supply applications, the digital level should be CMOS levels from VSS to VDD. In dual supply systems, the digital level should be CMOS levels from GND to VDD. The PWR pin should be connected to VSS or VDD.

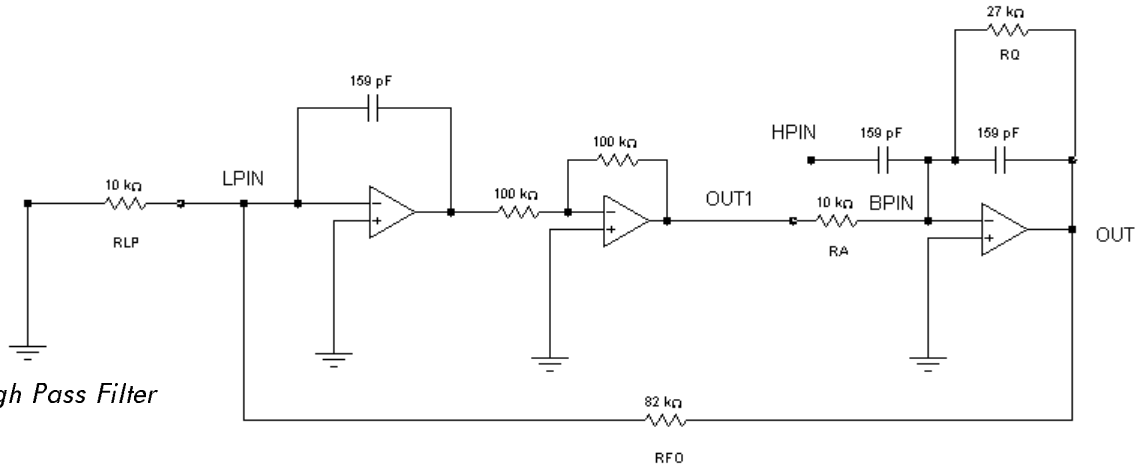
Typical Application Circuits



Low Pass Filter



Band Pass Filter



High Pass Filter