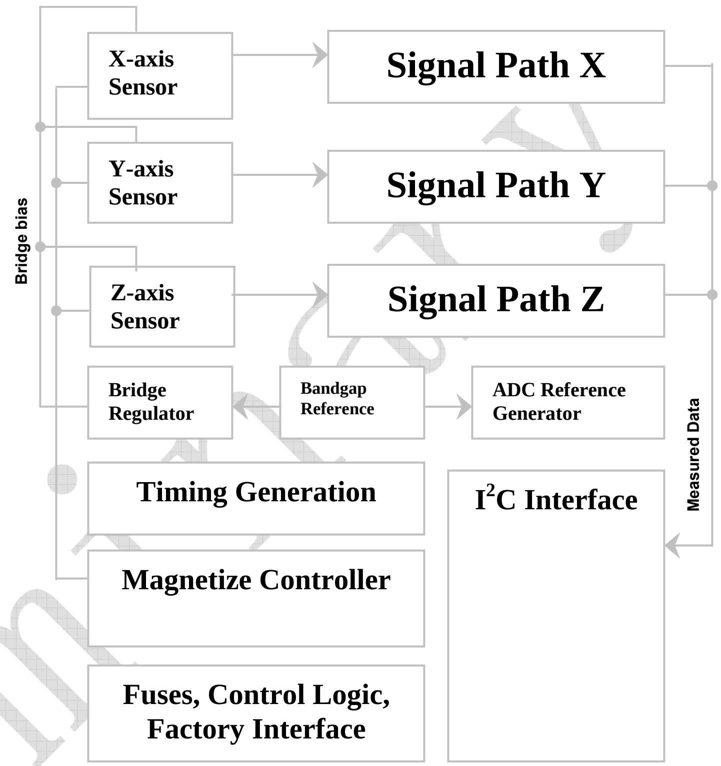
Ultra Small 3-axis Magnetic Sensor, With I²C Interface

MMC328xMS

FEATURES

- Full integration of 3-axis magnetic sensors and electronics circuits resulting in less external components needed
- Flexible output resolution available, up to 14bits
- Small Low profile package 3.0x3.0x1.0mm
- Low power consumption
- Power up/down function available through I²C interface
- With continuous operation mode, frequency selectable
- I²C Slave, FAST (≤400 KHz) mode
- 1.8V compatible IO
- 1.62V~3.6V wide power supply operation supported
- RoHS compliant



FUNCTIONAL BLOCK DIAGRAM

APPLICATIONS :

Electronic Compass
GPS Navigation
Position Sensing
Magnetometry

DESCRIPTIONS :

The MMC328xMS is a 3-axis magnetic sensor, it is a complete sensing system with on-chip signal processing and integrated I²C bus, allowing the device to be connected directly to a microprocessor eliminating the need for A/D converters or timing resources. It can measure magnetic field with a full range of ±8 gausses.

The MMC328xMS is packaged in an ultra small low profile LGA package (3.0 x 3.0 x 1.0 mm) and is available in operating temperature ranges of -40°C to +85°C.

The MMC328xMS provides an I²C digital output with 400 KHz, fast mode operation.

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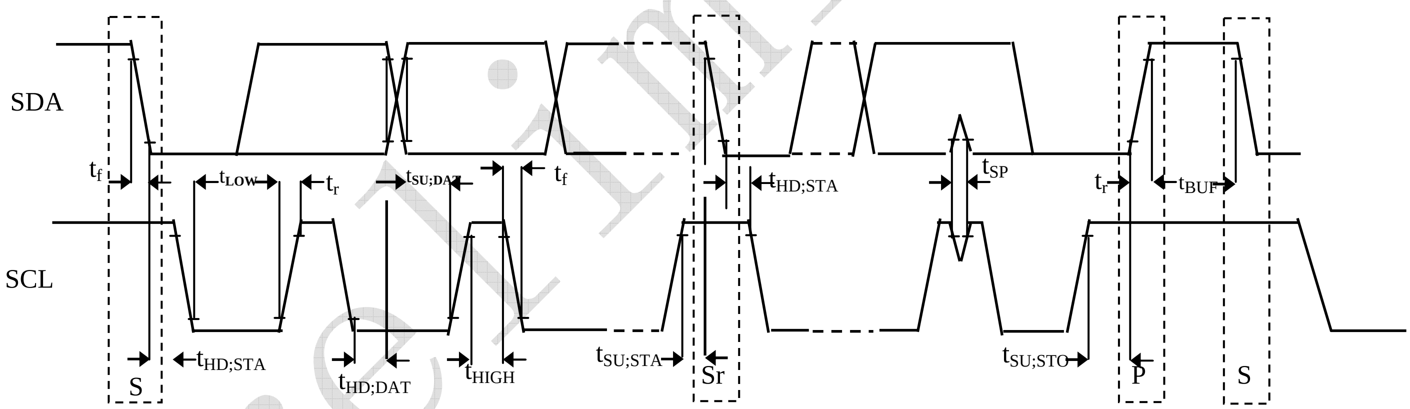
SPECIFICATION: (Measurements @ 25°C, unless otherwise noted; V_{DA} = V_{DD}= 3.0V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Field Range (Each Axis)	Total applied field	-8.0		+8.0	gauss
Supply Voltage	V_{DA}	1.62[1]	3.0	3.6	V
	V_{DD} (I^2C interface)	1.62[1]	3.0	3.6	V
Supply Current	50 measurements/second		0.55		mA
Power Down Current				1.0	µA
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
Linearity Error (Best fit straight line)	±1 gauss		0.1		%FS
	±4 gauss		1.0		%FS
	+4~+8guass -4~-8guass		5.0		%FS
Hysteresis	3 sweeps across ±4 gauss		0.1		%FS
Repeatability Error	3 sweeps across ±4 gauss		0.1		%FS
Alignment Error			±1.0	±3.0	degrees
Transverse Sensitivity			±2.0	±5.0	%
Total RMS Noise	1~25Hz, RMS		600		µgauss
Accuracy[2]			±2.0	±5.0	degrees
Bandwidth			25		Hz
Sensitivity	±4 gauss	-10		+10	%
		461	512	563	counts/gauss
Sensitivity Change Over Temperature	-40~85°C ±4 gauss		±1100		ppm/°C
Null Field Output	±4 gauss	-0.2		+0.2	gauss
Null Field Output Change Over Temperature[3]	Delta from 25°C ±4 gauss		±0.4		mgauss/°C
Disturbing Field		10			gauss
Maximum Exposed Field				10000	gauss

Note: [1]: 1.62V is the minimum operation voltage, or V_{DA} / V_{DD} should not be lower than 1.62V.
[2]: Accuracy is dependent on system design, calibration and compensation algorithms used.
The specification is based upon using the MEMSIC evaluation board and associate software.
[3]: It can be significantly improved when using MEMSIC's proprietary software or algorithm.

I^2C INTERFACE I/O CHARACTERISTICS (V_{DD}=3.0V)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	V_{IL}		-0.5		0.3* V_{DD}	V
Logic Input High Level	V_{IH}		0.7*V_{DD}		V_{DD}	V
Hysteresis of Schmitt input	V_{hys}		0.2			V
Logic Output Low Level	V_{OL}				0.4	V
Input Leakage Current	I_i	$0.1V_{DD}<V_{in}<0.9V_{DD}$	-10		10	µA
SCL Clock Frequency	f_{SCL}		0		400	kHz
START Hold Time	$t_{HD;STA}$		0.6			µS
START Setup Time	$t_{SU;STA}$		0.6			µS
LOW period of SCL	t_{LOW}		1.3			µS
HIGH period of SCL	t_{HIGH}		0.6			µS
Data Hold Time	$t_{HD;DAT}$		0		0.9	µS
Data Setup Time	$t_{SU;DAT}$		0.1			µS
Rise Time	t_r	From V_{IL} to V_{IH}			0.3	µS
Fall Time	t_f	From V_{IH} to V_{IL}			0.3	µS
Bus Free Time Between STOP and START	t_{BUF}		1.3			µS
STOP Setup Time	$t_{SU;STO}$		0.6			µS



Timing Definition

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) ………………...-0.5 to +5.0V
Storage Temperature …………….-55°C to +125°C
Maximum Exposed Field ………………..10000 gauss

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description: LGA-10 (3x3x1mm) Package

Pin	Name	Description	I/O
1	GND	Connect to Ground	P
2	Vpp	Factory Use Only, Leave Open	NC
3	V_{DA}	Power Supply	P
4	CAP	Connect to External Capacitor	I
5	TEST	Factory Use Only, Leave Open/No Connect	NC
6	V_{DD}	Power Supply for I^2C bus	P
7	SDA	Serial Data Line for I^2C bus	I/O
8	SCL	Serial Clock Line for I^2C bus	I
9	NC	No Connection	NC
10	NC	No Connection	NC

All parts are shipped in tape and reel packaging with 5000pcs per 13"reel.

Caution: ESD (electrostatic discharge) sensitive device.

Ordering Guide:
MMC328xMS

Package type:

Code	Type
S	LGA10 5050 pad arrangement RoHS compliant

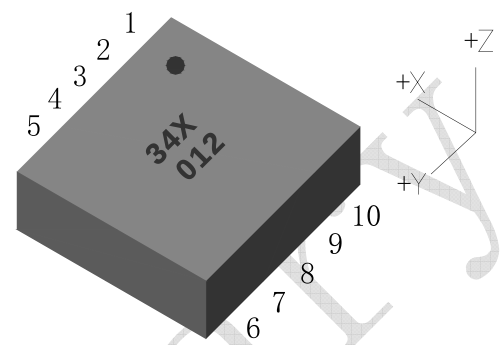
Performance Grade:

Code	Performance Grade
M	Temp compensated

Address code: 0~7

Code	7bit I^2C Address
0	0110000b
1	0110001b
2	0110010b
3	0110011b
4	0110100b
5	0110101b
6	0110110b
7	0110111b

Marking illustration:



Number 34X	Part number
340	MMC3280MS
341	MMC3281MS
342	MMC3282MS
343	MMC3283MS
344	MMC3284MS
345	MMC3285MS
346	MMC3286MS
347	MMC3287MS

Small circle indicates pin one (1).

THEORY:

The anisotropic magnetoresistive (AMR) sensors are special resistors made of permalloy thin film deposited on a silicon wafer. During manufacturing, a strong magnetic field is applied to the film to orient its magnetic domains in the same direction, establishing a magnetization vector. Subsequently, an external magnetic field applied perpendicularly to the sides of the film causes the magnetization to rotate and change angle. This in turn causes the film's resistance to vary. The MEMSIC AMR sensor is included in a Wheatstone bridge, so that the change in resistance is detected as a change in differential voltage and the strength of the applied magnetic field may be inferred.

However, the influence of a strong magnetic field (more than 10 gausses) along the magnetization axis could upset, or flip, the polarity of the film, thus changing the sensor characteristics. The MEMSIC magnetic sensor can provide an electrically-generated strong magnetic field to restore the sensor characteristics.

PIN DESCRIPTIONS:

V_{DA} – This is the supply input for the circuits and the magnetic sensor. The DC voltage should be between 1.62 and 3.6 volts. Refer to the section on PCB layout and fabrication suggestions for guidance on external parts and connections recommended.

GND – This is the ground pin for the magnetic sensor.

SDA – This pin is the I^2C serial data line, and operates in FAST (400 KHz) mode.

SCL– This pin is the I^2C serial clock line, and operates in FAST (400 KHz) mode.

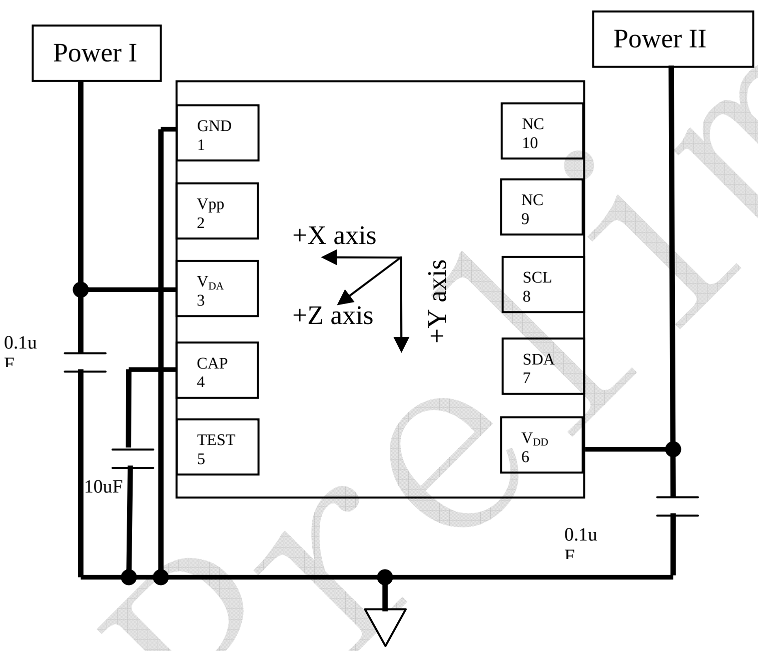
V_{DD} – This is the power supply input for the I^2C bus, and is 1.8V compatible can be 1.62V to 3.6V.

TEST – Factory use only, Leave Open/No Connect.

CAP –Connect a 10uF low ESR ceramic capacitor.

Vpp – Factory use only, Leave Open

EXTERNAL CAPACITOR CONNECTION



(Top View)

POWER CONSUMPTION

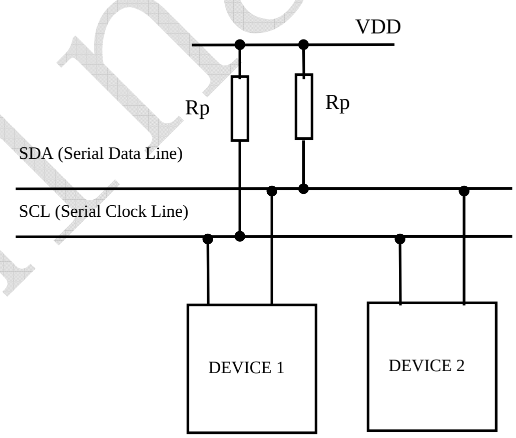
The MEMSIC magnetic sensor consumes 0.55mA (typical) current at 3V with 50 measurements/second, but the current is proportional to the number of measurements carried out, for example, if only 20 measurements/second are performed, the current will be 0.55*20/50=0.22mA.

I^2C INTERFACE DESCRIPTION

A slave mode I^2C circuit has been implemented into the MEMSIC magnetic sensor as a standard interface for customer applications. The A/D converter and MCU functionality have been added to the MEMSIC sensor, thereby increasing ease-of-use, and lowering power consumption, footprint and total solution cost.

The I^2C (or Inter IC bus) is an industry standard bi-directional two-wire interface bus. A master I^2C device can operate READ/WRITE controls to an unlimited number of devices by device addressing. The MEMSIC magnetic sensor operates only in a slave mode, i.e. only responding to calls by a master device.

I^2C BUS CHARACTERISTICS



I^2C Bus

The two wires in I^2C bus are called SDA (serial data line) and SCL (serial clock line). In order for a data transfer to start, the bus has to be free, which is defined by both wires in a HIGH output state. Due to the open-drain/pull-up resistor structure and wired Boolean “AND” operation, any device on the bus can pull lines low and overwrite a HIGH signal. The data on the SDA line has to be stable during the HIGH period of the SCL line. In other words, valid data can only change when the SCL line is LOW.

Note: Rp selection guide: 4.7Kohm for a short I^2C bus length (less than 4inches), and 10Kohm for less than 2inches I^2C bus.

REGISTER:

Register Name	Address	Description
Xout Low	00H	Xout LSB
Xout High	01H	Xout MSB
Yout Low	02H	Yout LSB
Yout High	03H	Yout MSB
Zout Low	04H	Zout LSB
Zout High	05H	Zout MSB
Status	06H	Device status
Internal control 0	07H	Control register 0
Internal control 1	08H	Control register 1
Residual0	1CH	Residual data after calibration
Residual1	1DH	Residual data after calibration
Residual2	1EH	Residual data after calibration
Residual3	1FH	Residual data after calibration
Residual4	20H	Residual data after calibration
Residual5	21H	Residual data after calibration

Register Details:

Xout High, Xout Low

Xout Low	7	6	5	4	3	2	1	0
Addr: 00H	Xout[7:0]							
Reset Value	Xout[7:0]							
Mode	R							

Xout High	7	6	5	4	3	2	1	0
Addr: 01H	Reserved		Xout[13:8]					
Reset Value	2'h0		Xout[13:8]					
Mode	R							

11 to 14bits X-axis output, 2's complement format.

Yout High, Yout Low

Yout Low	7	6	5	4	3	2	1	0
Addr: 02H	Yout[7:0]							
Reset Value	Yout[7:0]							
Mode	R							

Yout High	7	6	5	4	3	2	1	0
Addr: 03H	Reserved		Yout[13:8]					
Reset Value	2'h0		Yout[13:8]					
Mode	R							

11 to 14bits Y-axis output, 2's complement format.

Zout High, Zout Low

Zout Low	7	6	5	4	3	2	1	0
Addr: 04H	Zout[7:0]							
Reset Value	Zout[7:0]							
Mode	R							

Zout High	7	6	5	4	3	2	1	0
Addr: 05H	Reserved		Zout[13:8]					
Reset Value	2'h0		Zout[13:8]					
Mode	R							

11 to 14bits Z-axis output, 2's complement format.

Status:

Device Status	7	6	5	4	3	2	1	0
Addr: 06H	Reserved					NVM_Rd Done	Pump On	Meas Done
Reset Value	5'h0					0	0	0
Mode	R							

Register Name	Description
Meas Done	Indicates measurement event is completed, should be checked before reading output
Pump On	Indicates the charge pump status
NVW_Rd Done	Indicates the chip was able to successfully read its NVW memory.

Internal Control 0:

Control Register 0	7	6	5	4	3	2	1	0
Addr: 07H	Reserved		RM	No Boost	CM Freq1	CM Freq0	Cont Mode On	TM
Reset Value	2'h0		0	0	0	0	0	0
Mode	W	W	W	W	W	W	W	W

Register Name	Description
TM	Take measurement, set '1' will initiate measurement.
Cont Mode On	Set '1', the device will go into continuous operation mode
CM Freq0	Continuous operation mode frequency: 00: 50Hz, 01: 20Hz, 10: 10Hz; 11: 1Hz
CM Freq1	
No Boost	Set '1', the external capacitor will be charged directly from VDD (>2.5V).
RM	Set "1" will electrically magnetize the MR.

Internal Control 1:

Control Register 1	7	6	5	4	3	2	1	0
Addr: 08H	Reserved		Filt Time Sel1	Filt Time Sel0	Res Sel1	Res Sel0	FSR1	FSR0
Reset Value	2'h0		0	0	0	0	0	0
Mode	W	W	W	W	W	W	W	W

Register Name	Description
FSR0	Operation range selection, 00/11 +/-2Gausses; 01: +/-5 Gausses; 10: +/-4Gausses
FSR1	
Res Sel0	Output Data resolution selection, 00: 11bits; 01: 12bits; 10: 13bits; 11: 14bits
Res Sel1	
Filt Time Sel0	Select the bandwidth and the time the device is averaging the signal before going into A/D conversion, 00: 0.8mS; 01: 1.6mS; 10: 2.4mS; 11: 3.2mS.
Filt Time Sel1	

Residual0, Residual1, Residual2, Residual3, Residual4, Residual5

Residual0	7	6	5	4	3	2	1	0
Addr: 1CH	Residual0[7:0]							
Reset Value	Residual0[7:0]							
Mode	R							

Residual1	7	6	5	4	3	2	1	0
Addr: 1DH	Residual1[7:0]							
Reset Value	Residual1[7:0]							
Mode	R							

Residual2	7	6	5	4	3	2	1	0
Addr: 1EH	Residual2[7:0]							
Reset Value	Residual2[7:0]							
Mode	R							

Residual3	7	6	5	4	3	2	1	0
Addr: 1FH	Residual3[7:0]							
Reset Value	Residual3[7:0]							
Mode	R							

Residual4	7	6	5	4	3	2	1	0
Addr: 20H	Residual4[7:0]							
Reset Value	Residual4[7:0]							
Mode	R							

Residual5	7	6	5	4	3	2	1	0
Addr: 21H	Residual5[7:0]							
Reset Value	Residual5[7:0]							
Mode	R							

DATA TRANSFER

A data transfer is started with a “START” condition and ended with a “STOP” condition. A “START” condition is defined by a HIGH to LOW transition on the SDA line while SCL line is HIGH. A “STOP” condition is defined by a LOW to HIGH transition on the SDA line while SCL line is HIGH. All data transfer in I^2C system is 8-bits long. Each byte has to be followed by an acknowledge bit. Each data transfer involves a total of 9 clock cycles. Data is transferred starting with the most significant bit (MSB). After a “START” condition, master device calls specific slave device, in our case, a MEMSIC device with a 7-bit device address “**[0110xxx]**”. To avoid potential address conflict, either by ICs from other manufacturers or by other MEMSIC device on the same bus, a total of **8 different addresses** can be pre-programmed into MEMSIC device by the factory. Following the 7-bit address, the 8^{th} bit determines the direction of data transfer: [1] for READ and [0] for WRITE. After being addressed, available MEMSIC device being called should respond by an “Acknowledge” signal, which is pulling SDA line LOW.
In order to read sensor signal, master device should operate a WRITE action with a code of [xxxxxxx1] into MEMSIC device 8-bit internal register. Note that this action also serves as a “wake-up” call.

After writing code of [xxxxxxx1] into Internal Control 0, and the bit0 TM (Status Register, bit 0) is ‘1’, also a “READ” command is received, the MEMSIC device being called transfers 8-bit data to I^2C bus.

POWER DOWN MODE

MEMSIC MR sensor will enter power down mode automatically after data acquisition is finished.

EXAMPLE OF TAKE MEASUREMENT

First cycle: START followed by a calling to slave address [0110xxx] to WRITE (8^{th} SCL, SDA keep low). [xxx] is determined by factory programming, total 8 different addresses are available.

Second cycle: After an acknowledge signal is received by master device (MEMSIC device pulls SDA line low during 9^{th} SCL pulse), master device sends “[00000111]” as the target address to be written into. MEMSIC device should acknowledge at the end (9^{th} SCL pulse).

Third cycle: Master device writes to Internal Control Register 1 the code “[00000001]” as a wake-up call to initiate a data acquisition. MEMSIC device should send acknowledge.

A STOP command indicates the end of write operation.

Fourth cycle: Master device sends a START command followed by calling MEMSIC device address with a WRITE (8^{th} SCL, SDA keep low). An acknowledge should be send by MEMSIC device at the end.

Fifth cycle: Master device writes to MEMSIC device a “[00000110]” as the address to read.

Sixth cycle: Master device calls MEMSIC device address with a READ (8^{th} SCL cycle SDA line high). MEMSIC device should acknowledge at the end.

Seventh cycle: Master device cycles SCL line, the Status Register data appears on SDA line. Continuous read till Meas Done bit was set to ‘1’.

Eighth cycle: Master device sends a START command followed by calling MEMSIC device address with a WRITE (8^{th} SCL, SDA keep low). An acknowledge should be send by MEMSIC device at the end.

Ninth cycle: Master device writes to MEMSIC device a “[00000000]” as the address to read.

Tenth cycle: Master device calls MEMSIC device address with a READ (8^{th} SCL cycle SDA line high). MEMSIC device should acknowledge at the end.

Eleventh cycle: Master device continues to cycle the SCL line, next byte of internal memory should appear on SDA line (LSB of X channel). The internal memory address pointer automatically moves to the next byte. Master acknowledges.

Twelfth cycle: MSB of X channel.

Thirteenth cycle: LSB of Y channel.

Fourteenth cycle: MSB of Y channel.

Fifteenth cycle: LSB of Z channel.

Sixteenth cycle: MSB of Z channel.

Master ends communications by NOT sending ‘Acknowledge’ and also followed by a ‘STOP’ command.

EXAMPLE OF MAGNETIZATION

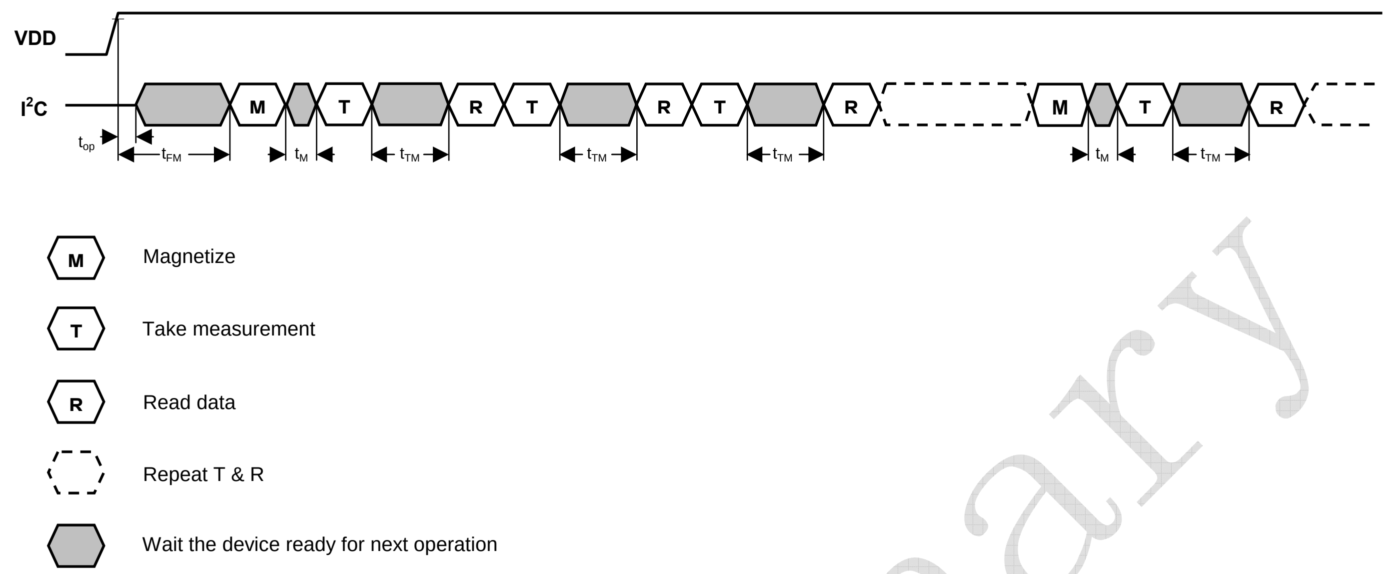
First cycle: START followed by a calling to slave address [0110xxx] to WRITE (8^{th} SCL, SDA keep low). [xxx] is determined by factory programming, total 8 different addresses are available.

Second cycle: After an acknowledge signal is received by master device (MEMSIC device pulls SDA line low during 9th SCL pulse), master device sends “[00000111]” as the target address (Internal Control Register 0). MEMSIC device should acknowledge at the end (9th SCL pulse).

Third cycle: Master device writes to internal MEMSIC device memory the code “[00100000]” as a wake-up call to initiate a magnetization action. MEMSIC device should send acknowledge.

A minimal of 50us wait should be given to MEMSIC device to finish magnetization action before taking a measurement. The RM bit will be automatically clear to “0” after magnetization is done. And the device will go into sleep mode afterwards.

OPERATING TIMING



Operating Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
Time to operate device after Vdd valid	t_{op}			20	µS
Wait time from power on to RM command	t_{FM}	10			mS
Time to finish magnetization	t_M	50			µS
Time to measure magnetic field	t_{TM}	7			mS

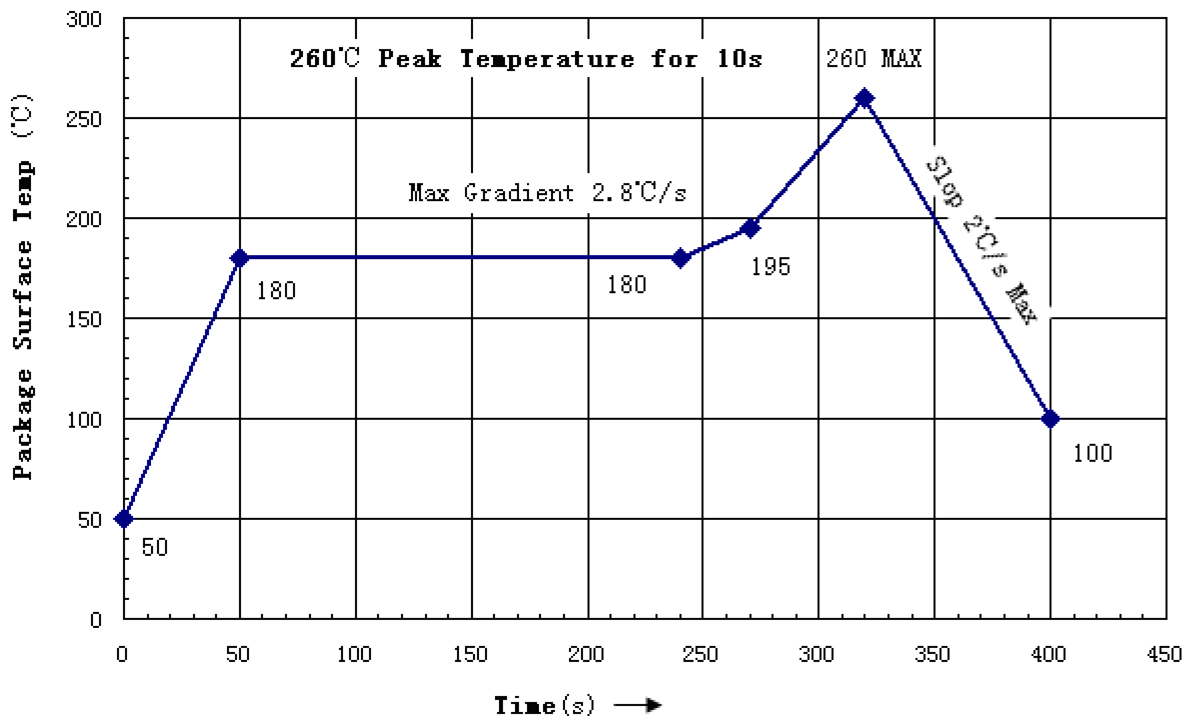
STORAGE CONDITIONS

Temperature: <30℃
Humidity: <60%RH
Period: 1 year (after delivery)

Moisture Sensitivity Level: 2
Bake Prior to Reflow: storage period more than 1 year, or humidity indicator card reads >60% at 23±5℃
Bake Procedure: refer to J-STD-033
Bake to Soldering: <1 week under 30℃/60%RH condition

SOLDERING RECOMMENDATIONS

MMC328xMS is capable of withstanding an MSL2 / 260℃ solder reflow. Following is the reflow profile:

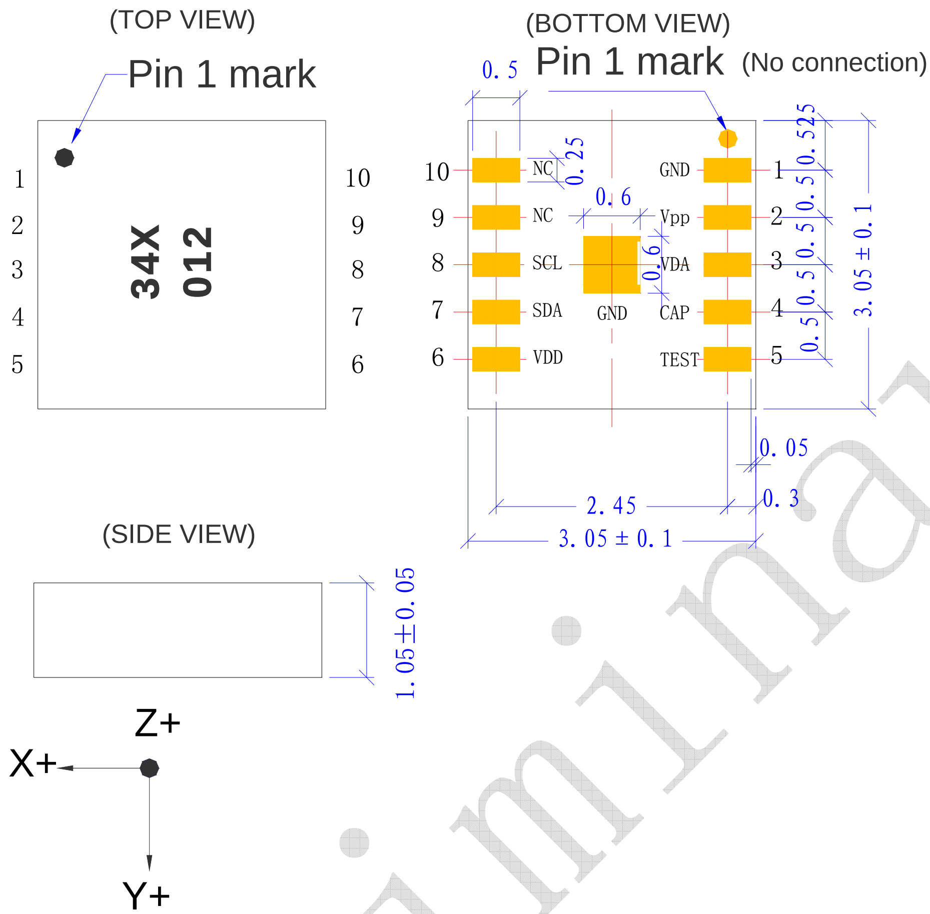


Note:

- Reflow is limited by 2 times
- The second reflow cycle should be applied after device has cooled down to 25℃ (room temperature)
- This is the reflow profile for Pb free process
- The peak temperature on the sensor surface should be limited under 260℃ for 10 seconds.
- Solder paste's reflow recommendation can be followed to get the best SMT quality.

If the part is mounted manually, please ensure the temperature could not exceed 260℃ for 10 seconds.

PACKAGE DRAWING



LAND PATTERN

The recommended land pattern is the same as the sensor’s solder pad. Please refer to the package drawing.