6/2002

Selectable Highpass/Notch Filter Data Sheet

MSHN1/MSHN2/MSHN3/MSHN4/MSHN5/MSHN6

Description

The selectable highpass/notch filter IC Is a CMOS chip that can be configured for either a highpass or a notch filter. The highpass response can be an 8 pole Butterworth, a 7 pole Elliptic or an 8 pole Bessel filter. The notch response can be narrow, wide or deep.The device uses switched-capacitor filters and no external components (except for decoupling capacitors) are required, Only an external CMOS level clock is needed. An on-chip lowpass filter is included to reduce output noise. The -3dB point is at approximately 0.2 of the clock frequency.

A four input multiplexor and externally selectable gain setting pin, along with a power down and clock to corner ratio select pin are included in the 16 pin version. An 8 pin version is also available for PC board area savings. Typical current consumption is as low as 200 uA and the minimum operating voltage is 2.7 volts, making the device ideal for portable applications. MSHN3, MSHN4 and MSHN6 are low current, lower frequency versions.

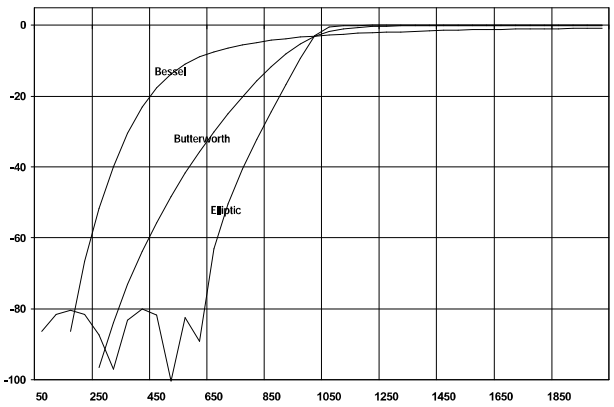
Features

Six Filter Types In One Package
No External Components
Switched-Capacitor Filters
Low Power Operation
Low Voltage Operation
Input Multiplexor
Adjustable Gain 0, 10 or 20 dB
Small Package Size
Low Cost
On Chip Power Save Pin

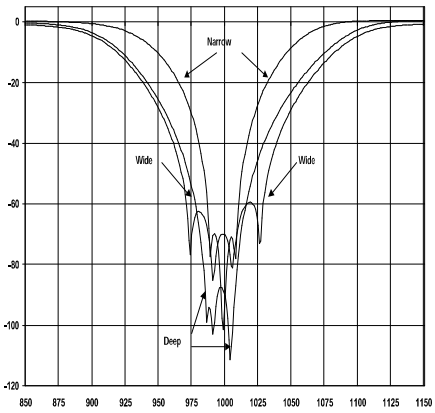
Applications

General Purpose Systems
Portable Systems
Telecommunications
Tracking Filters
Harmonic Analysis
Noise Analysis
Data Communication
Wireless Applications

Highpass Responses



Notch Responses



Electrical Characteristics

(VDD = +5.0V, T = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		2.7	5	5.5	V
Supply Current	IDD	MSHN1, MSHN2, MSHN5		1	1.5	mA
Supply Current	IDD	MSHN3, MSHN4, MSHN6		200	300	uA
Supply Current (Power Down)	IDD	MSHN2, MSHN4		100	200	uA
AC Specifications						
Gain	Av		-0.5	0	0.5	dB
Noise		To 1/2 Sample		250		uVrms
Distortion	THD	A weighted		-72		dB
Signal Swing		1 kHz	4	4.5		V p-p
Input Impedance	ZIN			1		Mohm
Output Drive	Io			1		mA
Output Impedance	Zo			500		ohm
Output Capacitive Load				50		pF
Clock to Corner		MSHN5, MSHN6	900	1000	1020	
Clock to Corner		MSHN1, MSHN3	99	100	101	
Clock to Corner		MSHN2, MSHN4, Fo=0	99	100	101	
Clock to Corner		MSHN2, MSHN4, Fo=1	900	1000	1020	
Center Frequency Range	Fo	MSHN1, MSHN2	0.001		20	kHz
Center Frequency Range	Fo	MSHN3, MSHN4	0.001		5	kHz
Center Frequency Range	Fo	MSHN5	0.001		2	kHz
Center Frequency Range	Fo	MSHN6	0.001		500	Hz
Ripple						
Elliptic Highpass				0.2		dB
Stop Band Rejection						
Elliptic/Butterworth Highpass				80		dB
-3 dB top Notch Bandwidth						
Narrow		Normalized Fo	0.92		1.08	
Wide		Normalized Fo	0.88		1.12	
Deep		Normalized Fo	0.89		1.11	
Bottom Notch Bandwidth						
Narrow		Normalized Fo	0.99	1.00	1.01	
Wide		Normalized Fo	0.97	1.00	1.03	
Deep		Normalized Fo	0.99	1.00	1.01	
Notch depth						
Narrow				-70		dB
Wide				-60		dB
Deep				-80		dB

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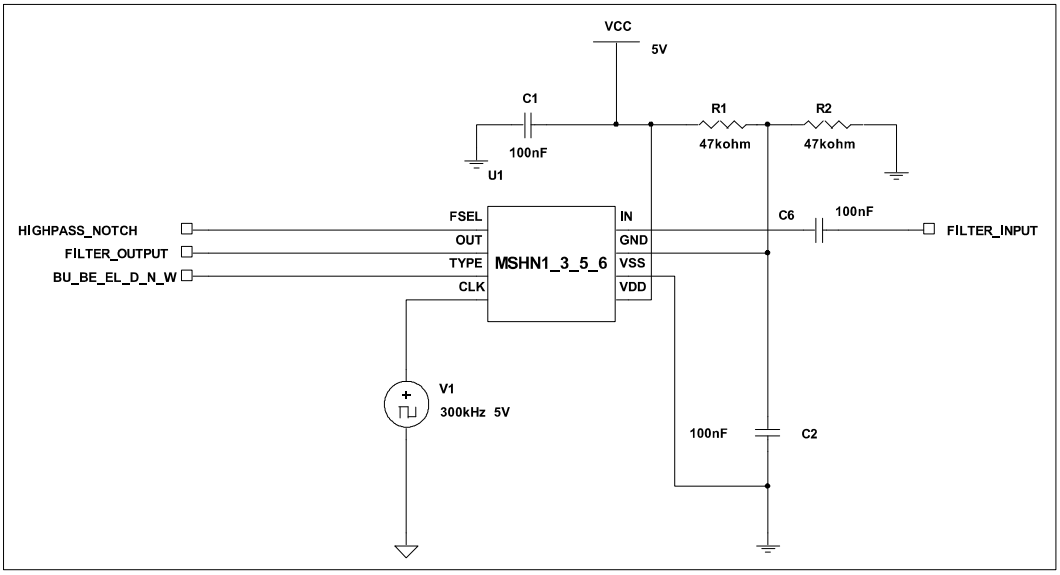
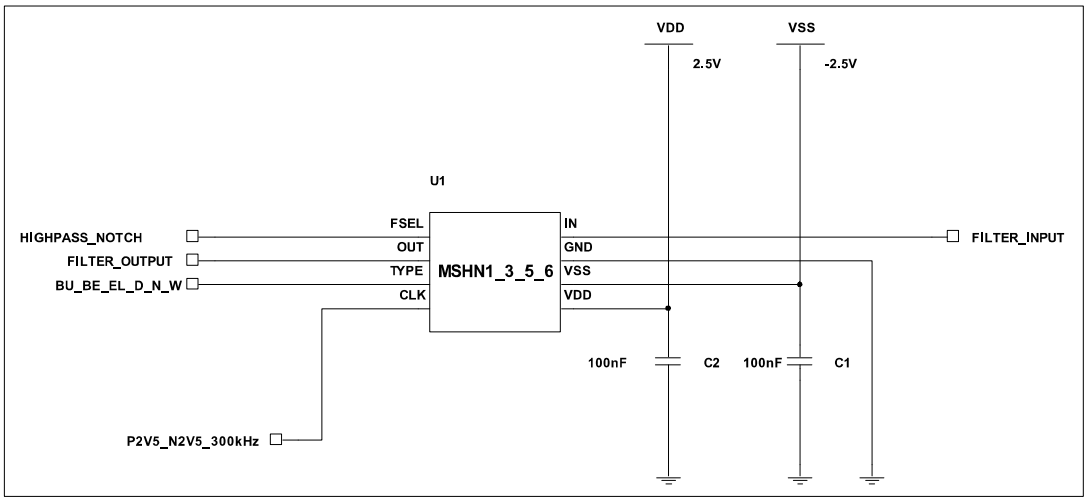
Application Schematics for MSHN1, MSHN3, MSHN5 and MSHN6



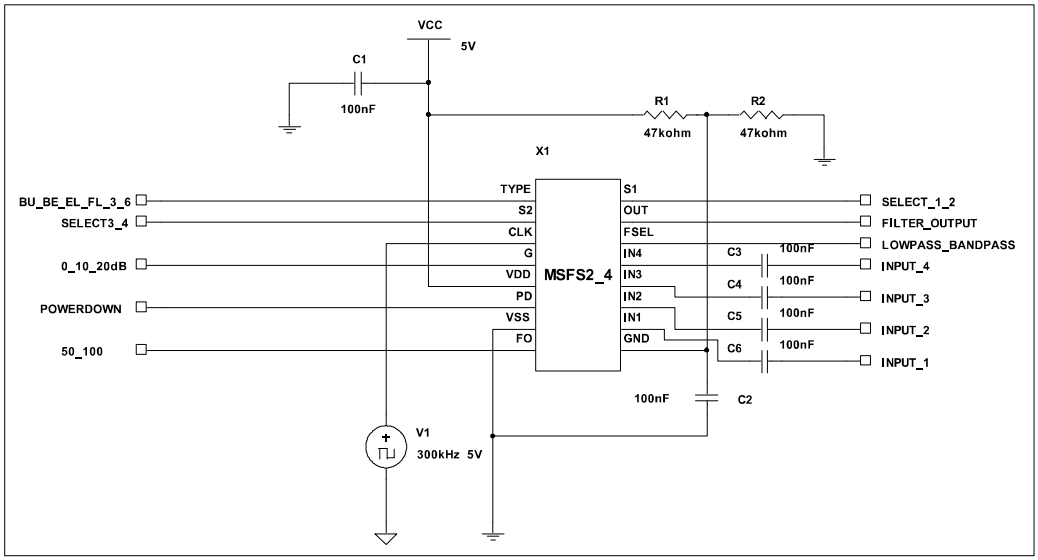
Single Supply



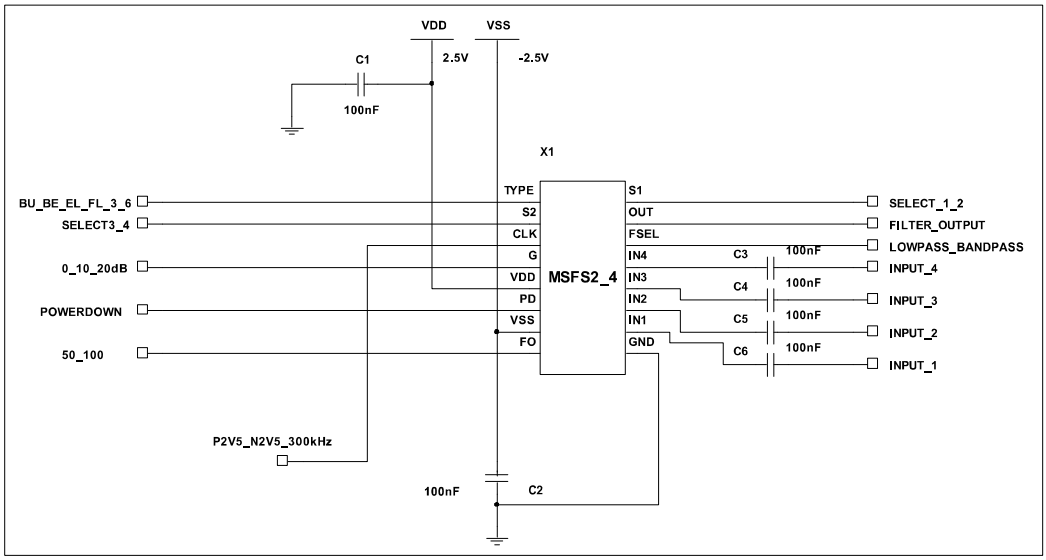
Dual Supply

Selectable Highpass/Notch Filter Data Sheet

Application Schematics for MSHN2 and MSHN4



Single Supply



Dual Supply

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Filter Selection

The filter type is selected using the two filter select pins, TYPE and FSEL, FSEL is a CMOS level pin that selects highpass or notch (highpass = 0, notch = 1). TYPE Is a tertiary control pin that selects the filter response. State 0 is VSS, state 1 is GND and state 2 is VDD.

TYPE	Highpass	Notch
0	Butterworth	Deep
1	Bessel	Narrow
2	Elliptic	Wide

Gain and Frequency Selection

The Gain control pin G is a tertiary control pin where state 0 is VSS, state 1 is GND level and state 2 is VDD.

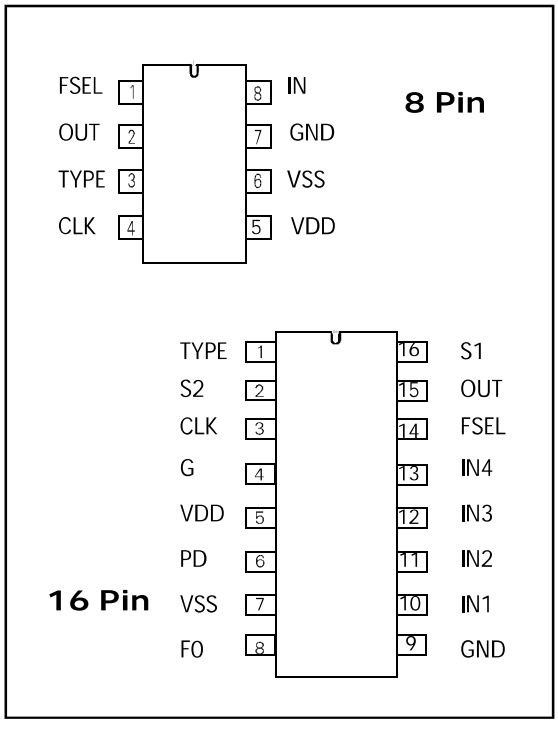
G	Gain
0	OdB
1	10dB
2	20dB

The frequency control pin F0 is a CMOS level pin where high is clock to corner of 1000 to 1 and low is clock to corner of 100 to 1.

Pin Description

1. TYPE — Filter Response Select Pin.
2. S2 — Input Multiplexor Select Pin
3. CLK — Clock Input
4. G — Gain Select Pin
5. VDD — Positive Power Supply, Typically 2.5 Volts for Split Supply 5.0 Volts for Single Supply
6. PD — Power Down Pin, CMOS level, Hi = Power Down
7. VSS — Negative Power Supply, Typically -2.5 Volts for Split Supply. 0 Volts for Single Supply
8. F0 — Clock to Corner Select Pin
9. GND — GND Pin, OV for Split Supplies 2.5 Volts Typical for Single Supply
10. IN1 — Input 1, Select Code 00
11. IN2 — Input 2, Select Code 01
12. IN3 — Input 3, Select Code 10
13. IN4 — Input 4, Select Code 11
14. FSEL — Selects Filter. O = High Pass, 1 = Notch
15. Out — Filter Output
16. S1 — Input Multiplexor Select Pin

Pin Configuration



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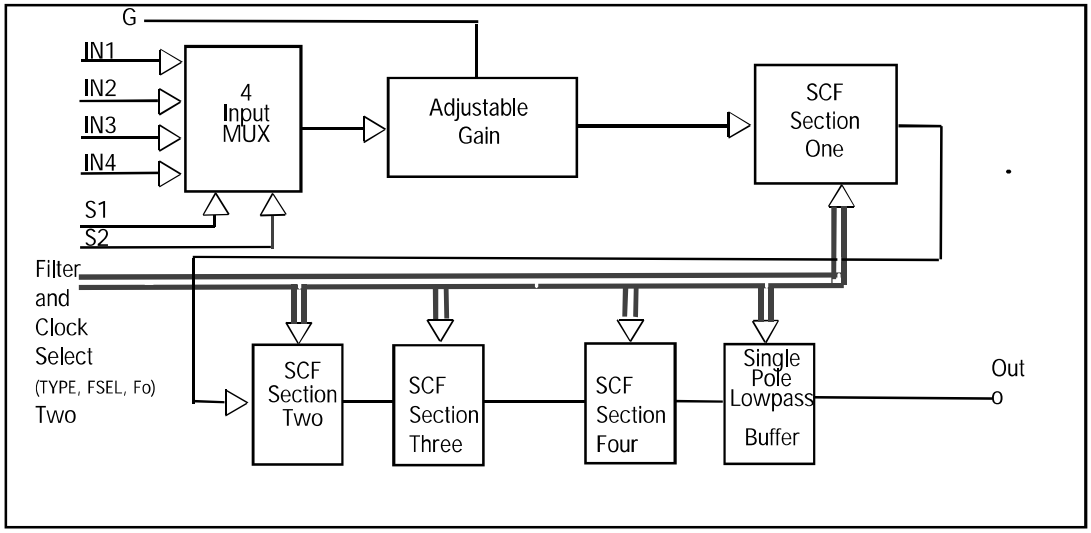
Block Diagram



Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature	-60 to +150 C
Operating Temperature	0 to 70 C

Ordering Information

Part Number	Package	Clock to Corner Ratio
MSHN1P	8 Pin DIP	100
MSHN2P	16 Pin DIP	100 or 1000
MSHN3P	8 Pin DIP	100
MSHN4P	16 Pin DIP	100 or 1000
MSHN5P	8 Pin DIP	1000
MSHN6P	8 Pin DIP	1000
MSHN1S	8 Pin SOIC	100
MSHN2S	16 Pin SOIC	100 or 1000
MSHN3S	8 Pin SOIC	100
MSHN4S	16 Pin SOIC	100 or 1000
MSHN5S	8 Pin SOIC	1000
MSHN6S	8 Pin SOIC	1000

Digital Levels

All the clock and control pins (except FSEL and G) are referenced between GND and VDD. In single supply applications, the digital levels should be CMOS levels from VSS to VDD. In dual supply systems, the digital levels should be CMOS levels from GND to VDD.

Input Selection

The input is selected using the Input Select Pins S1 and S2.

S2	S1	Input
0	0	1
0	1	2
1	0	3
1	1	4