6/2014

Selectable Low Voltage Lowpass/Bandpass Filter Data Sheet

MSLFS

Description

The selectable lowpass/bandpass filter IC Is a CMOS chip that can be configured for either a lowpass or a bandpass filter. The lowpass response can be a 7 pole Butterworth, Elliptic or Bessel filter. The band pass response can be a six pole full, third or sixth octave bandpass filter. The device uses switched-capacitor filters and no external components (except for decoupling capacitors) are required, Only an external clock is needed.

An externally selectable gain setting pin, a power down pin and clock to corner ratio select pin are included. Typical current consumption is as low as 500 uA and the minimum operating voltage is 1.0 volts, making the device ideal for portable applications. There is also an on chip op amp that can be used to provide additional gain.

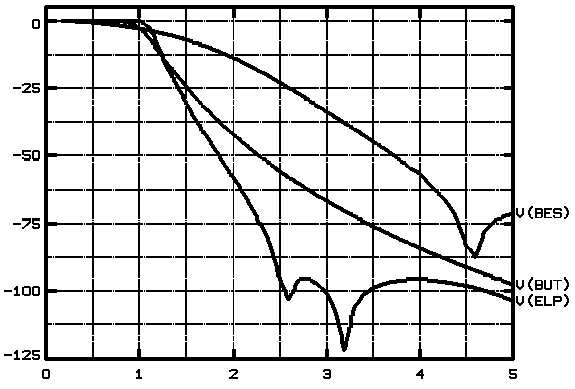
Features

Six Filter Types In One Package
No External Components
Switched-Capacitor Filters
Low Power Operation
Low Voltage Operation
Adjustable Gain 0, 6 or 12 dB
Small Package Size
Low Cost
On Chip Power Save Pin
ANSI Compatible Bandpass

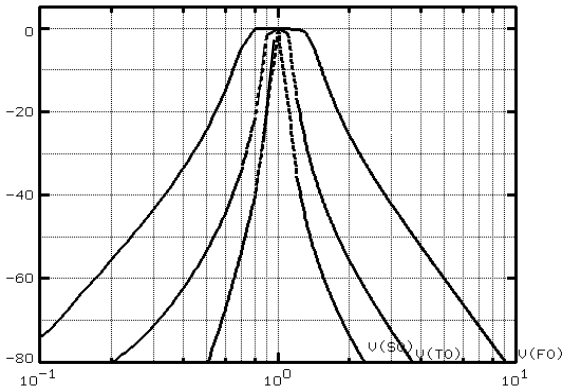
Applications

Spectrum Analyzers
General Purpose Systems
Portable Systems
Anti-Alias Filters
Reconstruction Filters
Telecommunications
Tracking Filters
Harmonic Analysis
Noise Analysis
Data Communication
Wireless Applications

Lowpass Responses



Bandpass Responses



Electrical Characteristics_____

(VDD = +1.2V, T = 25° C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Operating Voltage	VDD		1	1.2	3.6	V
Supply Current	IDD	VDD = 3.3V		1.5		mA
Supply Current	IDD	VDD = 1.0V		500		uA
Supply Current	IPD	Power Down, PD=1		50		uA
AC Specifications						
Gain	Av		-0.5	0	0.5	dB
Noise		To 1/2 Sample		250		uVrms
Distortion	THD			-62		dB
Signal Swing		1 kHz, VDD = 1.2V	800			mV p-p
Input Impedance	ZIN			1		Mohm
Output Drive	Io			1		mA
Output Impedance	Zo			500		ohm
Output Capacitive Load				22		pF
Clock to Corner *		Fo=1		85.3		Hz/Hz
Clock to Corner *		Fo=0		42.65		Hz/Hz
Center Frequency Range	Fo		0.001		6	kHz
Ripple						
Elliptic Lowpass				0.2		dB
Full Octave				0.2		dB
Third Octave				0.2		dB
Sixth Octave				0.2		dB
Stop Band Rejection						
Elliptic/Butterworth Lowpass		fCLOCK = 2.048 MHz		75		dB
Bessel Lowpass		fCLOCK = 2.048 MHz		65		dB
40 dB Bandwidth						
Full Octave		Normalized Fo	0.3		3	
Third Octave		Normalized Fo	0.6		1.67	
Sixth Octave		Normalized Fo	0.76		1.32	
Bandpass Q						
Full Octave Q	Q			1.5		
Third Octave	Q			4.5		
Sixth Octave	Q			9		

* External clock is 8X internal clock

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Filter Selection

The filter type is selected using the two filter select pins, TYPE and FSEL, FSEL is a pin that selects lowpass or bandpass (lowpass = 0, bandpass = 1). TYPE is a tertiary control pin that selects the filter response. State 0 is VSS, state 1 is GND and state 2 is VDD.

	FSEL=0	FSEL=1
TYPE	Lowpass	Bandpass
0	Butterworth	Full Octave
1	Bessel	Third Octave
2	Elliptic	Sixth Octave

Pin Description

1. TYPE	Filter Response Select Pin
2. GND	AC Ground, decouple with 0.1 uF to VSS
3. VREF	Reference Voltage, internally generated, typically VDD/2.2 for Single Supply Operation
4. MICIN	Input to Mic Amp
5. MICOUT	Output of Mic Amp
6. FO	Clock to Corner Select Pin
7. G	Gain Select Pin
8. FSEL	Selects Filter. 0 = Low Pass, 1 = Bandpass
9. VDD	Positive Power Supply, Typically 1.2 Volts for Single Supply
10. CTVL	Activate or Disable Boost Circuit
11. PD	Power Down Pin, CMOS level, Hi = Power Down
12. CLK	Clock Input
13. PWR	Sets Bias Current for Filter Stages, Lo=low power, Hi=normal power
14. OUT	Filter Output
15. VSSL	Bypass Capacitor for Boost Circuit, voltage at this pin is negative in relation to VSS, tie positive side of polarized cap to VSS
16. VSS	Ground Pin, 0 Volts for Single Supply

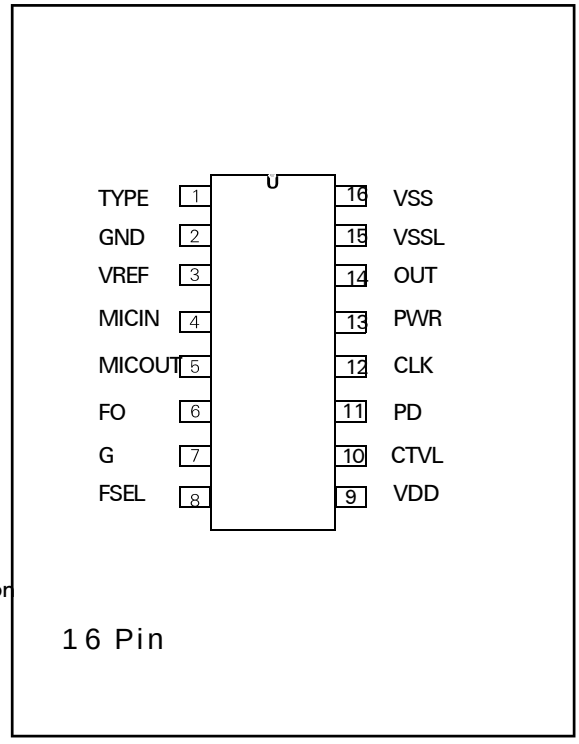
Gain and Frequency Selection

The Gain control pin G is a tertiary control pin where state 0 is VSS, state 1 is GND level and state 2 is VDD.

G	Gain
0	OdB
1	6dB
2	12dB

The frequency control pin F0 is a pin where high is clock to corner of 85.3 to 1 (170.6 to 1 for Bessel) and low is clock to corner of 42.65 to 1 (85.3 to 1 for Bessel).

Pin Configuration



16 Pin

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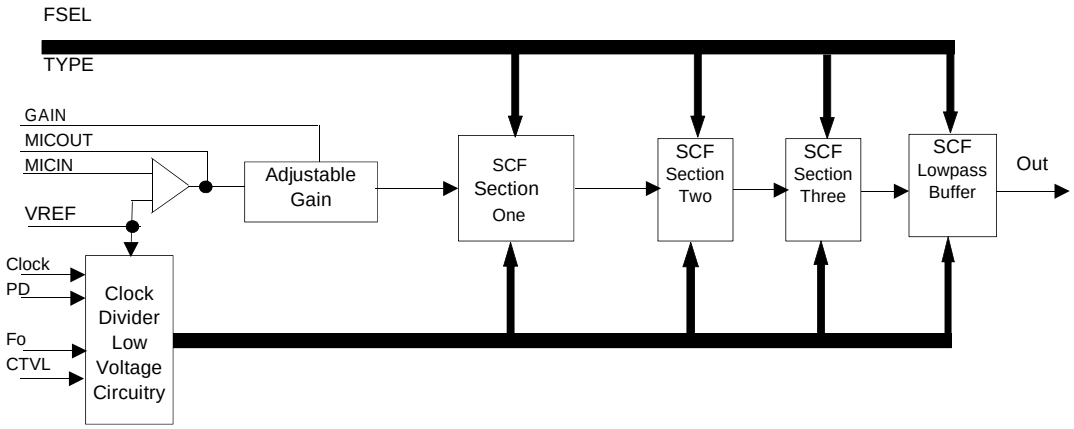
Block Diagram



Absolute Maximum Ratings

Power Supply Voltage	+5V
Storage Temperature	-60 to +150 C
Operating Temperature	0 to 70 C

Ordering Information

Part Number	Package
MSLFSP	16 Pin DIP
MSLFSS	16 Pin SOIC

Digital Levels

All the clock and control pins are referenced between VSS and VDD. In single supply applications, the digital levels should be CMOS levels from VSS to VDD. The tertiary controls (pins - TYPE and GAIN) should be set at VSS, VREF or VDD depending on the filter type or gain desired.

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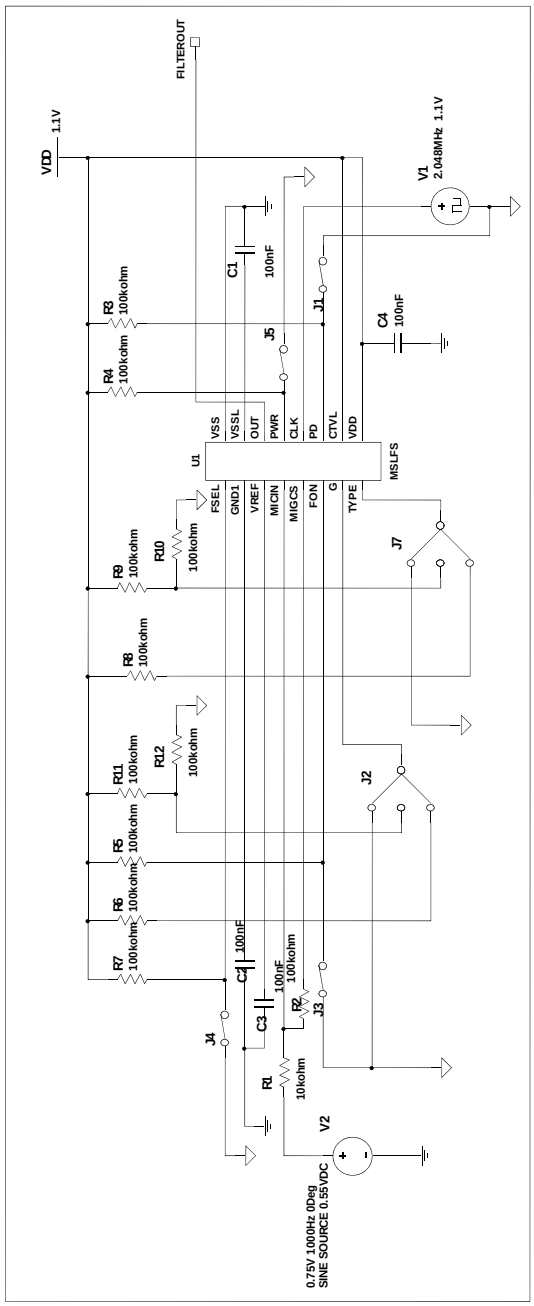
Typical Application Schematic



Notes

STANDARD PRODUCTS

MSRFIF	Radio Frequency Interface Front End
MSFIPS	FIPS-140 Level 4+ Security Supervisor
MSSCSA	Single Chip Spectrum Analyzer
MSTHDA	Total Harmonic Distortion Analyzer
MSLSA	Low Power Spectrum Analyzer
MSCPSI	Controller Programmable Sensor Interface
MSSPSI	Smart Programmable Sensor Interface
MSEPAF	Electrically Programmable Active Filter
MSCBT	Communications Baseband Transceiver
MSGEQ5A	Five Band Spectrum Analyzer
MSGEQ7	Seven Band Spectrum Analyzer
MSHFS1-6	Selectable High Frequency LP/BP Filter
MSFS1-6	Selectable Lowpass/Bandpass Filter
MSU1F1-4, MSU2F1	Resistor Programmable Universal Active Filter
MSU1HF1-4, MSU2HF1	High Frequency Resistor Programmable Universal Active Filter
MSELP	Switched Capacitor Elliptic Lowpass Filter with Op Amps
MSNBLP	Switched Capacitor Butterworth Lowpass Filter
MSLE/B/C5L/M	Switched Capacitor General Purpose Lowpass Filter
MS2LFS	Dual Selectable Low Voltage Lowpass/Bandpass Filter
MSLFS	Selectable Low Voltage Lowpass/Bandpass Filter
MSHN1-6	Selectable High Pass/Notch Filter
MSDET	Tone Detector

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