Preliminary

CBC921 PMRTC

New Product!

Data Brief

Real-Time Clock/Calendar with Power Manager and Battery Charger

Features

- Ultra-low power Real-Time Clock (RTC) with power-fail detect and battery management
- Low power timer and power manager extend run time in battery-powered systems
- Controls 4.1V rechargeable micro-batteries and 3.2V rechargeable coin cells and supercaps; no off-chip components required for battery charger
- Buck charge pump supply extends backup battery life:
  - 20nA RTC using internal RC oscillator
  - 50nA RTC using crystal oscillator
- Counters for hundredths, seconds, minutes, hours, date, month, year, century, and weekdays based on a 32.768KHz crystal oscillator or internal RC oscillator
- Automatic leap year calculation
- Alarm capability on all counters
- Two configurable multi-use outputs for interrupts, output clock, and managing sleep mode of external devices
- 64 bytes of RAM
- Internal temperature measurement with 10-bit ADC enables oscillator temperature compensation
- Advanced crystal calibration to ± 1 ppm
- Ultra-low Iq VIN POR circuit (< 25nA)
- Fixed indicators for PGOOD, charging current on, and charging disabled
- Temperature range -40°C to +85°C

Applications

- **Power bridging** to provide uninterruptible RTC function during exchange of main batteries.
- **Consumer appliances** that have real-time clocks; provides switchover power from main supply to backup battery.
- **Ultra-Low Power Timer** using only 20nA
- **Wireless sensors and RFID tags** and other powered, low duty cycle applications.
- **Business and industrial systems** such as: network routers, point-of-sale terminals, single-board computers, test equipment, multi-function printers, industrial controllers, and utility meters.
  - Reliable system timekeeping
  - Battery-powered devices
  - Internet of Things, portable devices
  - Daily alarms

3mm x 3mm x 0.5mm 16-pin MLPQ Package

General Description

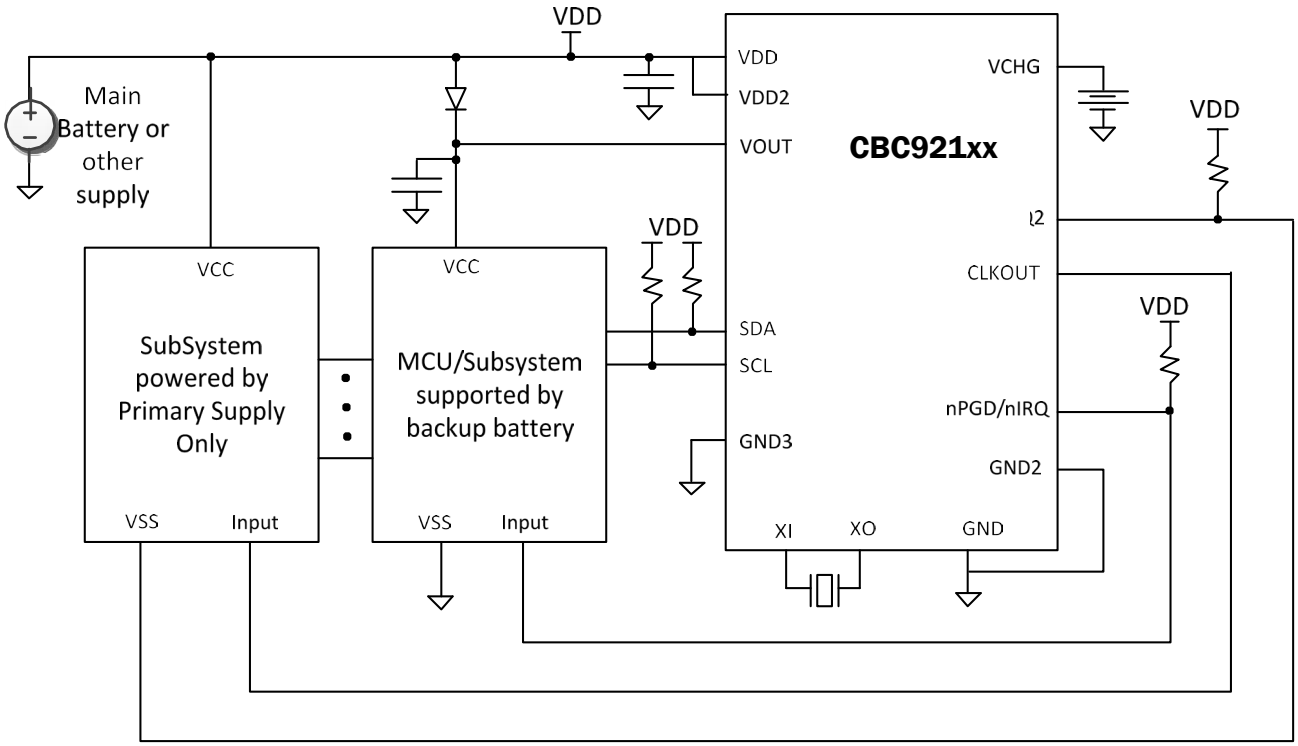
The CBC921xx combines a real-time clock (RTC) with a backup battery charger and other power management features. In the event of an outage of the primary power source, automatic switchover to the backup battery enables extended timekeeping and optionally provides power to external devices to maintain their operation during the power outage.

In normal operation the RTC function is supported by a primary power source, which can be a battery cell, multiple alkaline batteries, or a regulated power supply ranging from 2.85V to 5.5V. The backup battery is charged with a temperature-compensated voltage derived from the primary voltage source. The backup battery charging is refreshed with a configurable schedule and temperature-dependent duty cycle, both of which are designed to increase service life of the backup battery while minimizing power consumption from the main power source.

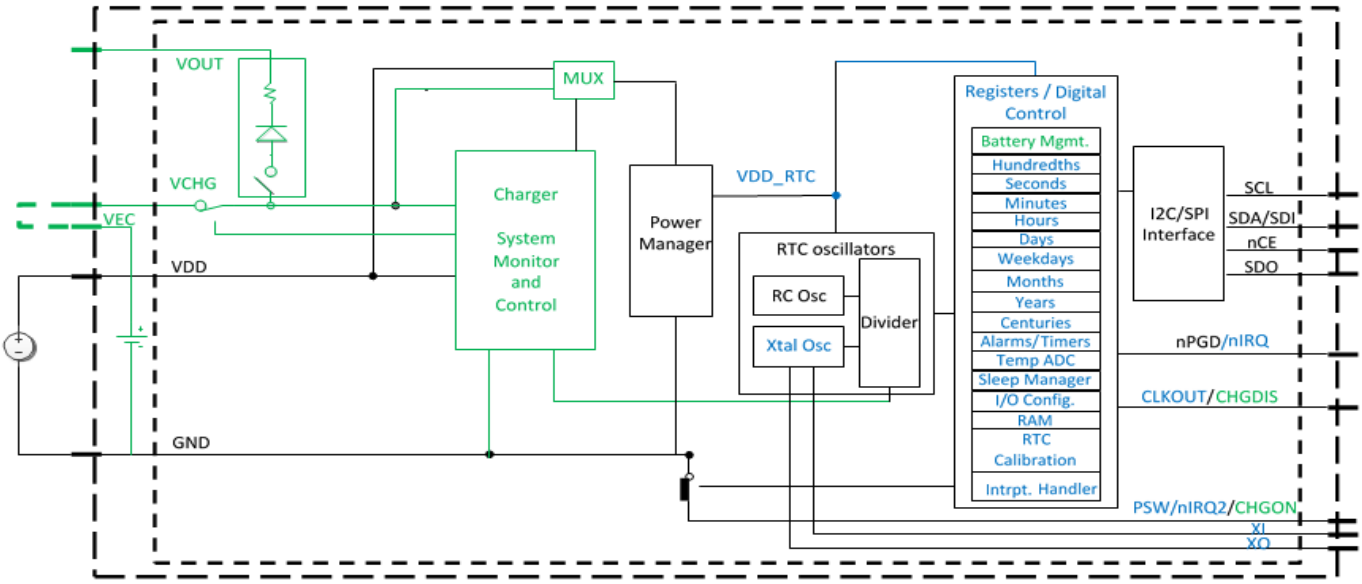
The circuit can be used in applications to provide an uninterrupted continuous time clock, calendar function, and time-based interrupts or alarms for wake up from sleep to active mode operation with adjustable intervals to save power in the overall system.

The power management has a low quiescent current and high efficiency for backup battery charging. The RTC circuit has very low quiescent current to extend the RTC run time. The RTC has 2ppm accuracy for clock, calendar, alarm, clock outputs, and interrupt functions. An open drain internal power switch is controlled by interrupts and a sleep manager to facilitate power saving by disconnecting main power from external devices according to user-defined schedules.

CBC921 Typical Application Schematic



Block Diagram



Pin Descriptions

Pin #	PM-RTC Pin	PM I²C	PM SPI	RTC I²C	RTC SPI	Pin Type	Pin Function (for PM-RTC versions with I²C or SPI)
1	XO	NC	NC	XO	XO	Analog output (high-Z)	Crystal oscillator connection high-impedance node. Minimize trace length between the crystal and the I.C.
2	VOUT	VOUT	VOUT	NC	NC	Supply Output	Output voltage providing bias to external circuits in backup mode only. Enabled by VOUTEN register bit. A high-resistance switch and series diode feeding this pin limit the output current and protect the battery.
3	GND2	GND2	GND2	GND2	GND2	ground	This pin must be connected to ground (GND).
4	GND	GND	GND	GND	GND	ground	Ground
5	nCE	GND3	nCE	GND3	nCE	Digital Input (CMOS)	Chip Enable for SPI. Connect this pin to ground when using the I²C version.
6	PSW/ nIRQ2	nCHGON	nCHGON	PSW /nIRQ2	PSW /nRQ2	Output - Open Drain	Configurable open-drain output. This pin has a low-resistance switch to ground which can be connected to the ground return of external devices to switch power to those devices. If no interrupt is enabled, PSWEN_WAKE=1, and no other function is configured by the Control Register 2, this pin has the default function of indicating with an active low output if the battery is currently being charged.
7	VCHG	VCHG	VCHG	NC	NC	Supply In/Out	Regulated voltage source output for backup battery charging. Power supply input in backup mode. Connect a battery or other energy storage device between this pin and GND.
8	SDA/ SDI	SDA	SDI	SDA	SDI	Digital I/O - Open Drain	Serial data input/output for I²C version. Serial data input for SPI version. A pull-up resistor is needed on this bus. A value between 5 KΩ and 100 KΩ is recommended depending on the clock frequency of the serial communications.

Pin Descriptions (continued)

							frequency of the serial communications.
9	SDO	NC	SDO	NC	SDO	Digital Output (CMOS)	Serial data output for SPI version. Leave this pin open when using I²C version.
10	SCL	SCL	SCL	SCL	SCL	Digital Input (CMOS)	I²C clock/SPI clock
11	nPGD /nIRQ	nPGD	nPGD	nPGD/ nIRQ	nPGD/ nIRQ	Output - Open Drain	Configurable PGOOD indicator and interrupt1 output. Initially functions as a power good signal, going to an active-low state when the SC63xxx I/O's are ready. At this time, the pin function may be reconfigured by writing to the OUT1S bit through the serial port. Otherwise, this pin will follow the PGOOD register bit, staying active-low until VDD falls below the POR falling threshold. A pull-up resistor to VDD is required to use this pin. Use a maximum value of 200 MΩ, but a lower value may be needed for higher frequency output selections.
12	CLK OUT	CHGDIS	CHGDIS	CLKOUT	CLKOUT	Digital Output - CMOS	Programmable CMOS clock output. Until configured by the clock output control register, this pin has the default function of indicating (with output high) if charging is disabled by either the CHGOFF or CHGRST register bits.
13	NC	NC	NC	NC	NC	open	Unused pin, not connected to the I.C.
14	VDD2	VDD2	VDD2	VDD2	VDD2	Supply	This pin must be connected to the VDD pin.
15	VDD	VDD	VDD	VDD	VDD	Supply	Main power source input. Can be connected to the main battery or another voltage source. Place decoupling capacitor of at least 0.1uF between VDD and GND close to the I.C.
16	XI	NC	NC	XI	XI	Analog input	Crystal oscillator input, high-impedance node. Minimize trace length between the crystal and the I.C.
17	EP	EP	EP	EP	EP	Exposed Pad	Connect the exposed pad to GND.

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
External Supply Input (VDD)	V_{DD} to V_{GND}	-0.3 to +6.0	V
Battery Connection Pin (VCHG)	V_{CHG} to V_{GND}	-0.3 to +4.15	V
Supply Output Voltage Pin (VOUT)	V_{OUT} to V_{GND}	-0.3 to +6.0	V
XI, XO pins in VDD Mode	V_{XT_VDD} to V_{GND}	-0.3 to V_{DD} +0.3	V
XI, XO pins in Backup Mode	V_{XT_BAT} to V_{GND}	-0.3 to V_{CHG} +0.3	V
VDD2 pin to VDD pin	V_{DD2} to V_{DD}	-0.3 to +0.3	V
GND2 pin to GND pin	V_{GND2} to V_{GND}	-0.3 to +0.3	V
SCL, SDA/SDI, PSW/nIRQ2, nPGD/IRQ, nCE pins	V_{IO1} to V_{GND}	-0.3 to +6.0	V
CLKOUT and SDO pins, in Backup and VDD Modes	V_{IO2} to V_{GND}	-0.3 to V_{DD} +0.3	V
PSW/nIRQ2 pin current	I_{PSW}	200	mA
ESD Protection Level (HBM), VCHG pin (1)	V_{CHG_ESD} to V_{GND}	TBD	kV
ESD Protection Level (HBM), all other pins (1)	V_{IO_ESD} to V_{GND}	2	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Notes:
Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1): Tested according to JEDEC standard JESD22-A114-B. No ESD protection is guaranteed on the VCHG pin.

Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Impedance (2)	$R_{\theta JA}$	50	°C/W

Notes:
(2): Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: T_J < 85°C, -40°C < T_A <+85 °C, VDD = 3.6 V, 1uF VDD to GND. Typical values are for T_A=+25 °C

Parameter	Symbol	Conditions	Min	Typ.	Max.	Units
Supply Range						
VDD Supply Voltage Range	Vdd		V_{POR_rising}		5.5	V
VDD Power-on Reset Rising Threshold	V_{POR_rising}	Backup to VDD mode entry threshold		2.7	2.85	V
VDD Power-on Reset Falling Threshold	$V_{POR\_falling}$	Battery backup entry threshold	2			V
VDD Power-on Reset Threshold Hysteresis	$V_{POR\_hysteresis}$	V_{POR_rising} - $V_{POR\_falling}$	90	125	170	mV
VDD POR rising indicator delay, from cutoff mode	Td_{PGD_cutoff}	Measured from VDD crossing V_{POR_rising} to the falling edge of the nPGD/nIRQ pin, VCHG=2.5V		300		ms
VDD POR rising indicator delay, from backup mode	Td_{PGD_backup}	Measured from VDD crossing V_{POR_rising} to the falling edge of the nPGD/nIRQ pin, VCHG=4V		80		ms
Battery Charging Delay Time	Td_{CHG_rising}	Measured from falling edge of the nPGD/nIRQ pin to rising edge of CHG pin.		40		ms
VOUT Cut-in Time Delay	Td_{VOUT_rising}	Measured from VDD crossing $V_{POR\_falling}$ threshold to the VOUT switch turn-on		1		ms
Supply Currents						
VCHG Supply Current, RC Mode, with Cutoff Monitor Inactive	I_{CHG_RC4}	Includes RTC operating in RC mode. 4.1V version. VCHG =4.1V. VDD=0 V.		20		nA
VCHG Supply Current, RC Mode, with Cutoff Monitor Inactive	I_{CHG_RC3}	Includes RTC operating in RC mode. 3.2V version. VCHG =3.2V. VDD=0V.		60		nA
VCHG Supply Current, XT Mode, with Cutoff Monitor Inactive	I_{CHG_XtalH}	Includes RTC operating in XTAL mode. 4.1V version. VCHG =4.1V. VDD=0V.		50		nA
VCHG Supply Current, XT Mode, with Cutoff Monitor Inactive	I_{CHG_Xtal3}	Includes RTC operating in XTAL mode. 3.2V version. VCHG =3.2V. VDD=0V.		150		nA
VCHG Supply Current, XT Mode, with Cutoff Monitor Active	$I_{CHG\_XtalMon}$	Includes RTC operating in XTAL mode. 4.1V version only. VCHG =4.1V, VDD=0V		350		nA
VDD Supply Current with Battery Charging	Idd_{Charge}	After POR rising. Excludes battery charging current, but including RTC in Xtal mode. nCE pin held at VDD. SDA/SDI and SCL pins held at VDD or GND. I²C bus inactive, other I/O's not switching.		4000		nA
VDD Supply Current with Battery Not Charging	$Idd_{NoCharge}$	After POR rising. RTC operating in XTAL mode. I²C bus inactive. Other I/O's static. nCE pin held at VDD. SDA/SDI and SCL pins held at VDD or GND. No load on CLKOUT/ CHGDIS. Logic outputs high (open-drain).		75		nA
VDD Supply Current in Backup Mode	Idd_{BkUp}	VDD=2.5V		25		nA
CHG leakage Current, Cutoff Mode	I_{CHG_Cutoff}	VHG=2.5V. VDD=0V. 4.1V version only		70		pA

Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Battery Charger						
Battery Charger Output Current	I_{CHG_charge}	VCHG=3V		50		uA
Battery Charger Output Voltage	$VCHG_{41}$	25°C, VDD> $V_{POR\_rising\_MAX}$, 4.1V version	4.025	4.075	4.1	V
Battery Charger Output Voltage	$VCHG_{32}$	25°C, VDD > $V_{POR\_rising\_MAX}$, 3.2V version	3	3.1	3.2	V
Battery Charger Output Voltage TC	$VCHG_{TC41}$	25°C to 85°C, 4.1V version		-2.2		mV/degC
Battery Charger Output Voltage TC	$VCHG_{TC32}$	25°C to 85°C, 3.2V version		-1.67		mV/degC
Battery Cutoff Threshold	$VCHG_{Cutoff}$	4.1V version only	2.7	3	3.3	V
Oscillator						
RC Oscillator Frequency	F_{RC}	Ta=25 °C		256		Hz
RC Oscillator Frequency Accuracy	F_{RC_TOL}	Without calibration; supply between 2.9V and 5.5V	-4		+4	%
Crystal oscillation frequency	F_{XO}			32768		Hz
Crystal Internal Load Capacitance	CL_{INT}			2.5		pF
Crystal Negative Resistance	R_{NEG}			520		kΩ
Interface Logic						
Logic Input High Threshold	V_{IH}	VDD=5.5V	1.6			V
Logic Input Low Threshold	V_{IL}	VDD=2.9V			0.4	V
Logic Output High Level	V_{OH}	CMOS outputs				V
Logic Output Low Level	V_{OL}	IL<3mA			0.4	V
Logic Input Leakage	I_{dig_leak}			< 1		nA
Switch on-Resistance						
PSW/nIRQ2/nCHGON Pull Down Resistance	R_{PSW}	I_load= 100mA		4		Ω
VOUT Switch Resistance	R_{VOUT}	V_{CHG}=4.1V, I_load= 1µA		1		MΩ
Serial Interface						
I²C Clock Frequency	F_{I2C}				400	kHz
SPI Clock Frequency	F_{SPI}				2000	kHz

Note
(1): See chart of charge voltage v.s temperature (Figure 3)

Ordering Information

Part Number	RTC	Power Management	I/F	Charge Voltage
CBC92100C	Y		I²C	
CBC92100P	Y		SPI	
CBC92032C		Y	I²C	3.2V
CBC92041C		Y	I²C	4.1V
CBC92032P		Y	SPI	3.2V
CBC92041P		Y	SPI	4.1V
CBC92132C	Y	Y	I²C	3.2V
CBC92141C	Y	Y	I²C	4.1V
CBC92132P	Y	Y	SPI	3.2V
CBC92141P	Y	Y	SPI	4.1V

CBC92XYYZ Part Numbering	
X	1=RTC included, 0=no RTC
YY	Maximum battery charging voltage (x10) 00=no battery management included
Z	C=I²C, P=SPI