Questa Check Connect offers a distinct approach for verifying interconnect integrity within designs. It facilitates scalable verification for extra-large System-on-Chips (SoCs) through automated and exhaustive formal analysis. The solution is designed for easy deployment, delivering unique capabilities for conclusive results in complex connectivity challenges that surpass traditional capacity limits. This innovative tool significantly reduces engineering efforts by a factor of 10x and ensures predictable verification within project timelines.
Questa Check Connect
Ensure complex interconnectivity meets intent and specification

Benefits
- Automated conversion of specification to formal checks
- Complete formal analysis and prove interconnect is not broken for complex SoC
- Easy to deploy with distinct flow from setup to signoff
- Derive static and dynamic connectivity specification directly from design
- Enhanced methodology exceeding capacity limitations of traditional flows
- Enable predictable verification with runtimes in project time boundaries
- Scalable to extra-large SoC
- Efficient specification and formal verification of 1M plus connections
- Automation throughout reduces engineering effort

Summary
Questa Check Connect presents a unique strategy to ensure the integrity of interconnects in designs. It simplifies scalable verification for extensive System-on-Chips (SoCs) through automated and comprehensive formal analysis. The tool is engineered for effortless implementation and provides unparalleled functionalities to achieve conclusive outcomes when tackling intricate connectivity issues that go beyond conventional capacity boundaries. This groundbreaking solution substantially minimizes engineering work by a factor of 10x and guarantees reliable verification results within project schedules.

How the application works
The Questa Check Connect app effectively handles both specification and verification challenges. Users have the flexibility to utilize detailed specifications presented in either CSV or TCL commands. These specifications serve as inputs, alongside the design's Register Transfer Language (RTL) description. Leveraging the specification input, the app autonomously generates formal checks that undergo verification through potent formal engines. Simplified debugging is facilitated for all formal checks that fail, thanks to the waveform debugger or the schematic debugger. The app further streamlines issue resolution with driver and load tracing of signals, providing a straightforward path to identifying the root cause. To enhance verification management, all checks can transition into a coverage database, which then becomes an input for the verification management tool.

Figure 1 Questa Check Connect flow diagram

Questa Check Connect supports the full spectrum of connectivity specifications:
- Direct connection
- Delayed connection
- Condition guarded connection
Additional Features

- Supported Platforms
  - Linux 64 bit: RHEL 6-7; SLES 12
  - Windows 64 bit: Server 2003/2008/2012, 7/8.x/10
- Design Language
  - Mixed language support: Verilog/SV/VHDL
  - RTL and netlist support
  - Verilog, EDIF and Liberty library cell support
- Focused Structural Debug
  - Automatic identification and report of connection break point
  - Automatic identification of candidate select conditions in connection multiplexing logic
- Fast compilation of multi-billion-gate SoCs, ASICs, FPGAs
- Scales to designs with over 1M connections
- Supports complex and deep connections with thousands of signals in a connection path
- Supports verification of routing of global signals (e.g., clock, reset, scan enable), I/O pad multiplexing, IP integration, and more
- Supports additional, custom analysis of signals and logic in connection path (e.g., to check power domains)
- Single and multiple conditional delayed connections
- Support for constant in connection
- Mutex and conditional mutex connection
- Support for macros, macro list and wildcards
- Support delay range in connections
- Support for multi-clock domain connection paths
- Support for rule-based connection generation

Questa Check Connect Explorer Utility

The Explorer utility addresses issues associated with specifications. Its purpose is to minimize the effort required for creating and maintaining specifications by extracting connectivity specifications directly from the design IP or System on Chip (SoC).

Regardless of whether it's a new design or an existing one, Questa Check Connect's Explorer utility expedites the process of generating specifications. It goes beyond mere connection checks, offering insights into essential design aspects and tracking breakpoints.

Items generated and report by Questa Check Connect Explorer utility

- **Check types**: direct connection, delayed connection, inverted connection, condition guarded connection, constant and conditional guarded constant, single and multiple conditional delayed connection, etc.
- **Design aspects**: primary ports, registers, constants, undriven wires, black-box ports, instance ports, etc.
- **Breakpoints**: primary ports, registers, constants, undriven and black-box ports.

Questa Check Connect XL use model

Questa Check Connect XL use model addresses both the specification and verification challenges. User can create and maintain an abstract, compact connectivity specification leveraging IP and module integration rules, naming conventions, wildcards, and global multiplexing conditions. The App automatically generates the detailed connectivity specification table. Crucially, delays, inversions of polarity, and full paths for source, destination, and multiplexing signals are automatically generated.

![Figure 2 Questa Check Connect XL use model](image-url)
This results in a dramatic reduction in engineering effort. In addition, proofs are clustered and optimized through learning strategies and automated abstractions that deliver conclusive results within acceptable runtime. Finally, failures can be debugged easily as the App reports localized path information to pinpoints the connection break point.

The following connectivity specifications are supported:

- Module and instance-based source/destination connection definition
- High-level definition of global select condition rules
- Automatic generation of detailed connectivity specification
- Automatic detection of inverted polarity, delays, and multiplexing logic within a connection path

The App supports the following proof algorithm features:

- Access to the most advanced formal proof engines and setting
- Dedicated connectivity proof algorithms leveraging unified structural and logic analysis
- Automated abstractions to reduce proof complexity
- Automated proof learning strategies to cluster and speed up checks of similar connections
- High performance parallel algorithms utilizing computer grid